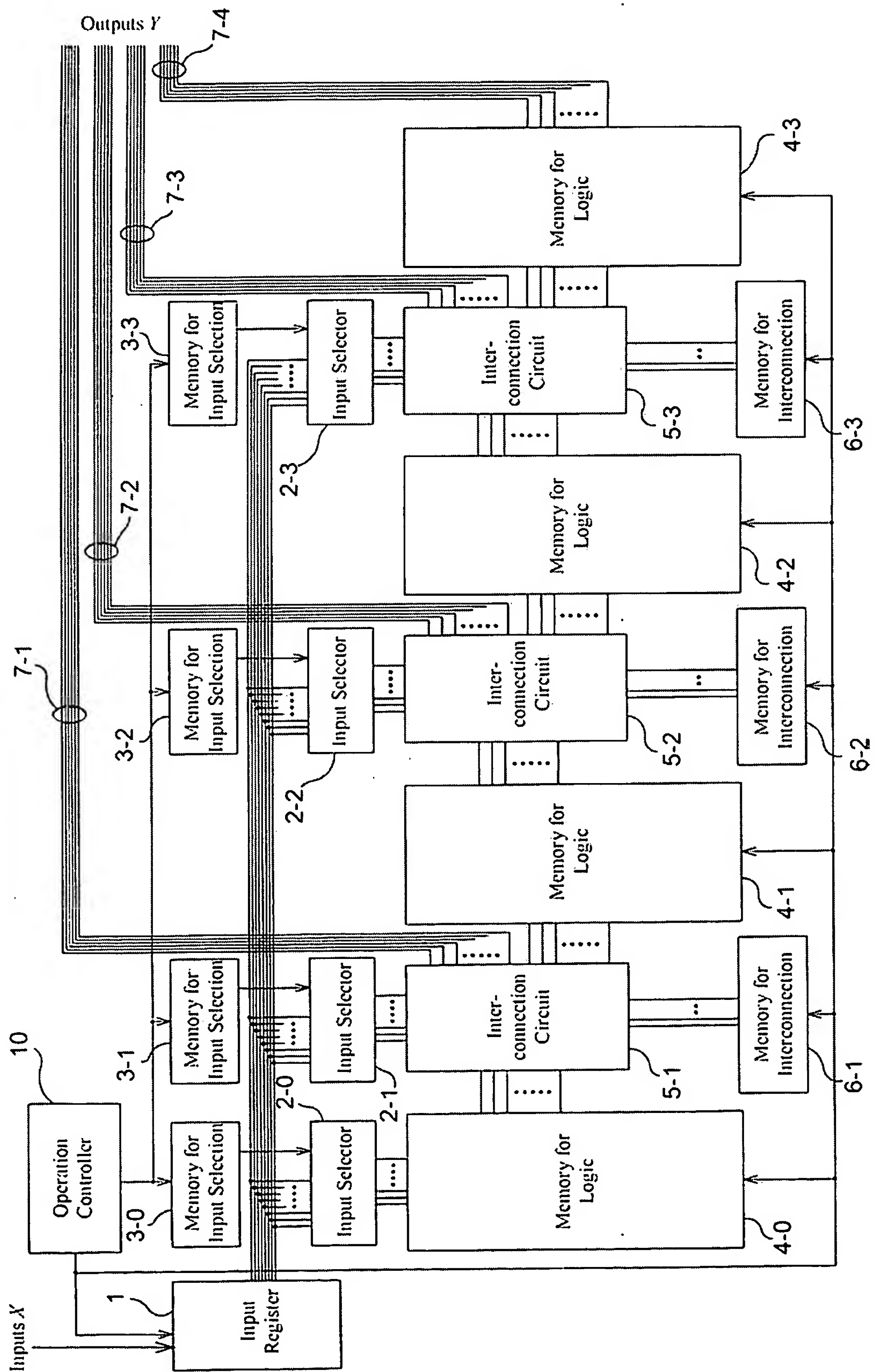


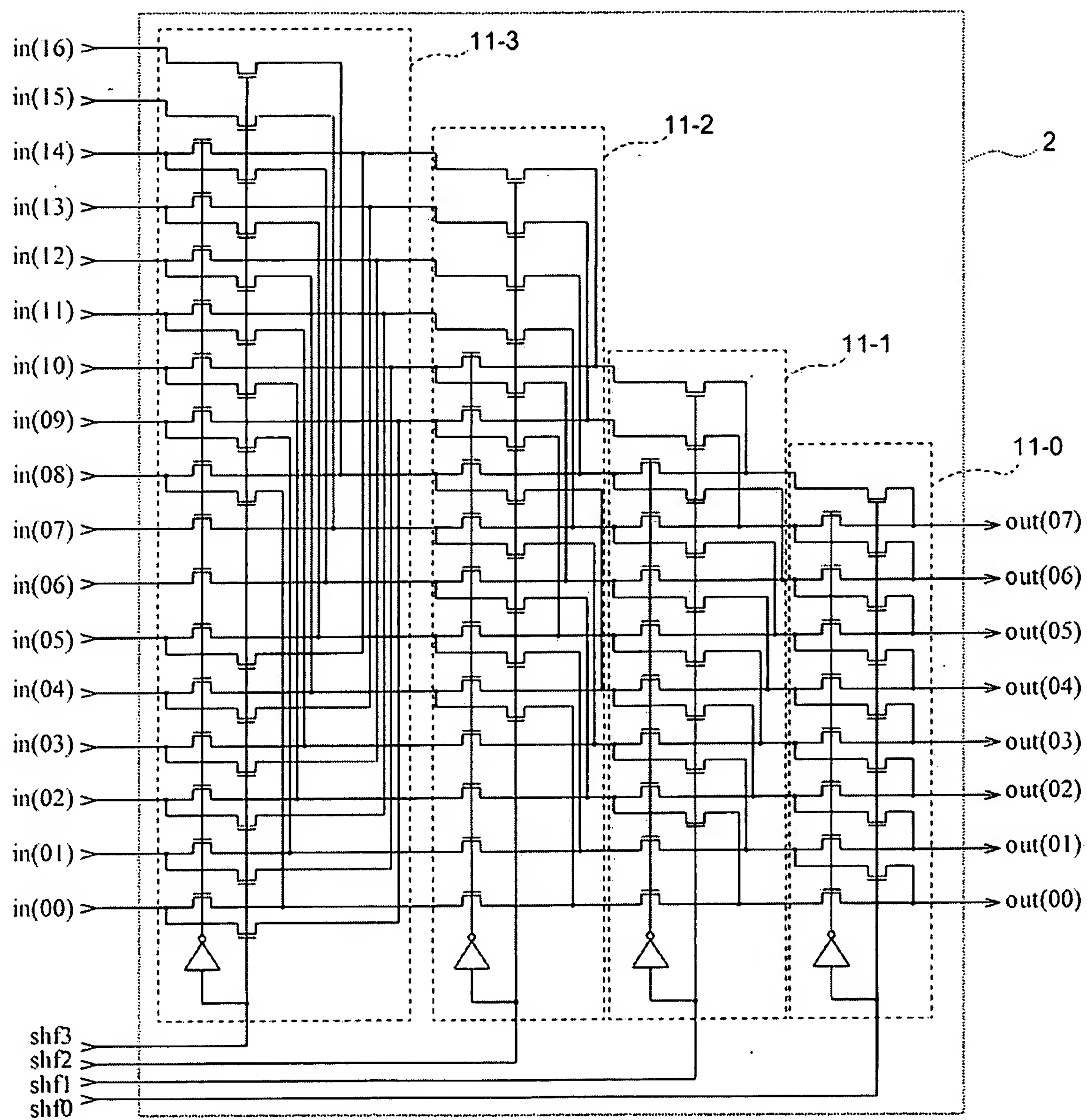
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FIG. 1



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FIG. 2



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FIG. 3

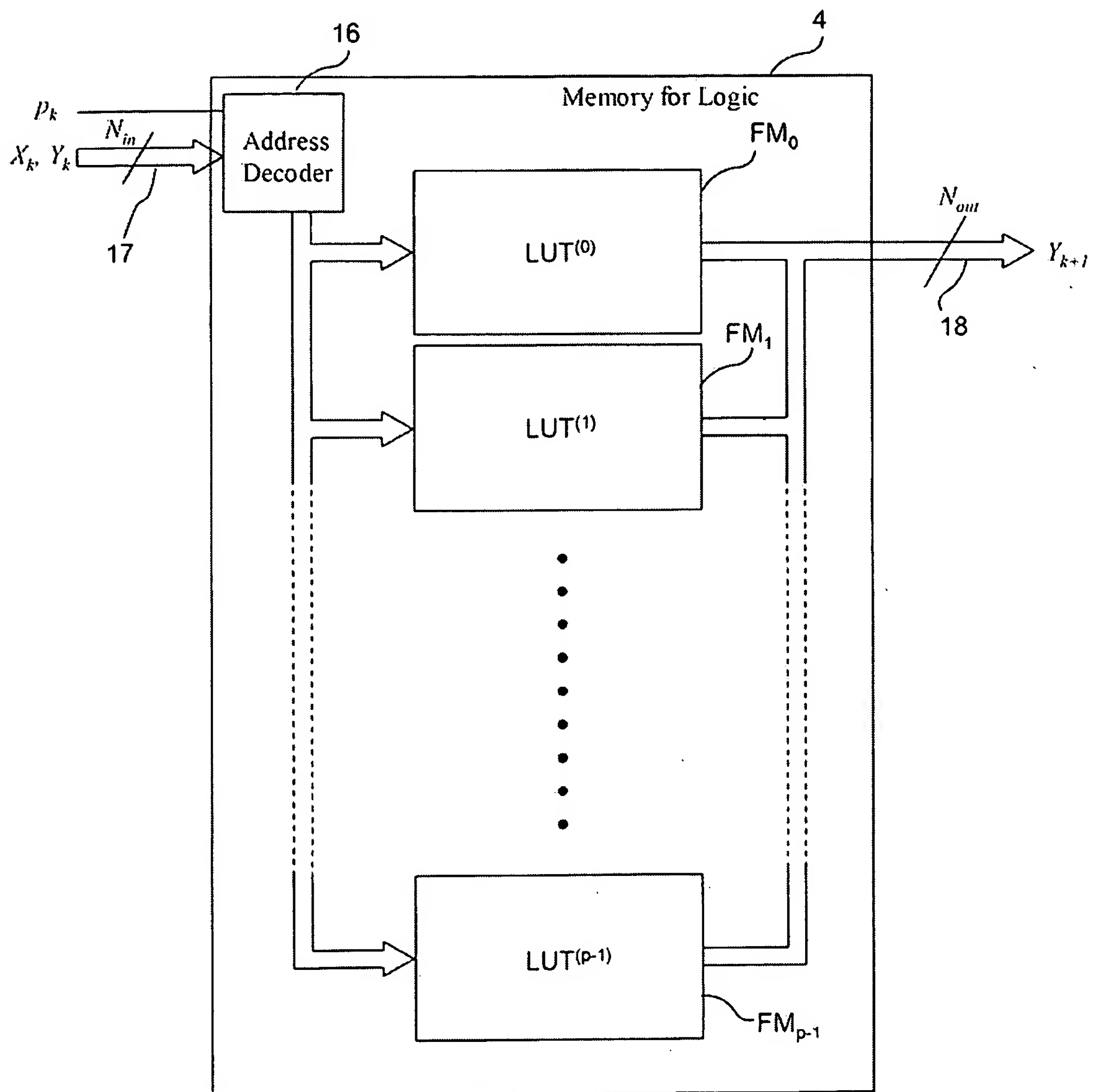
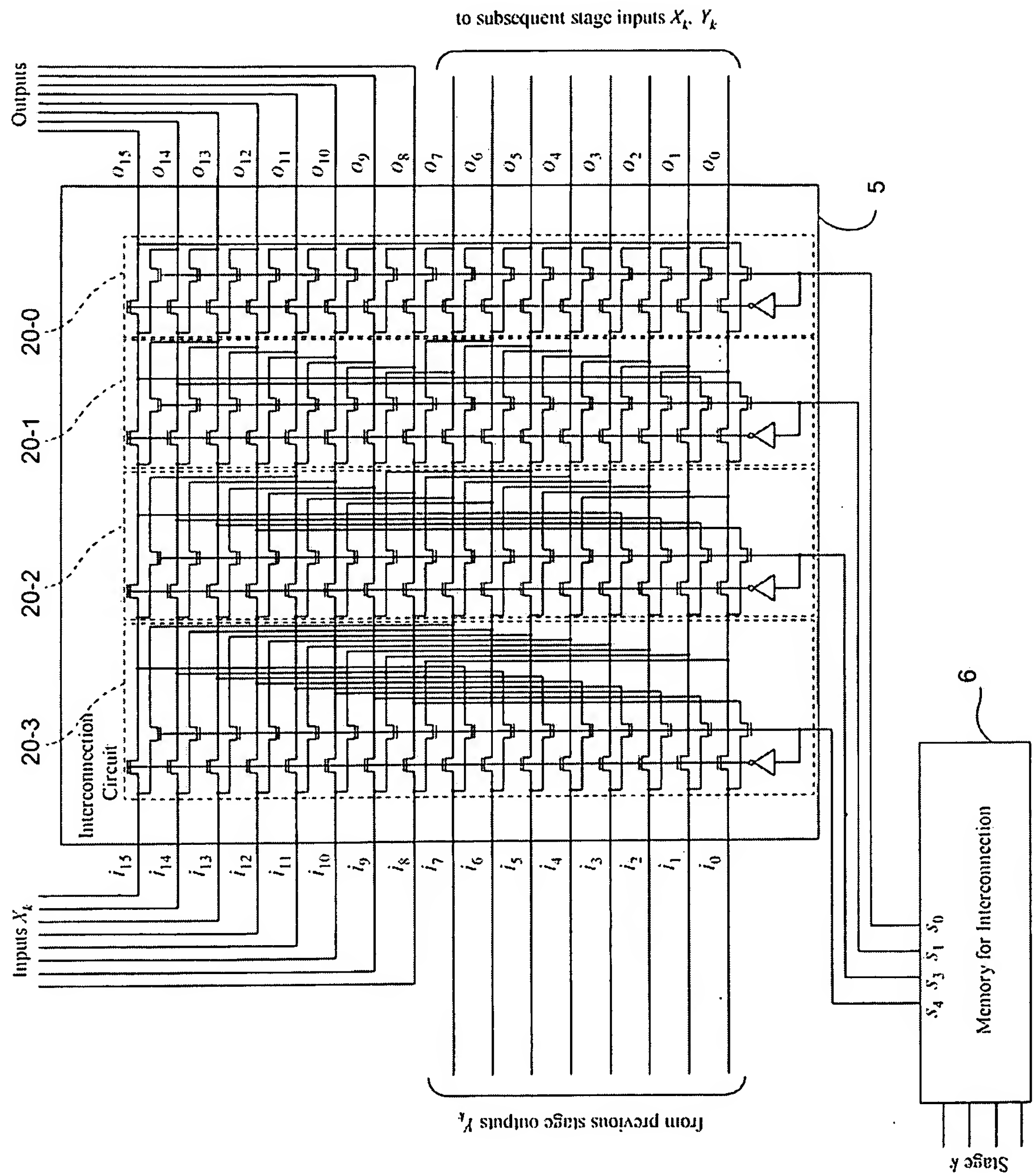
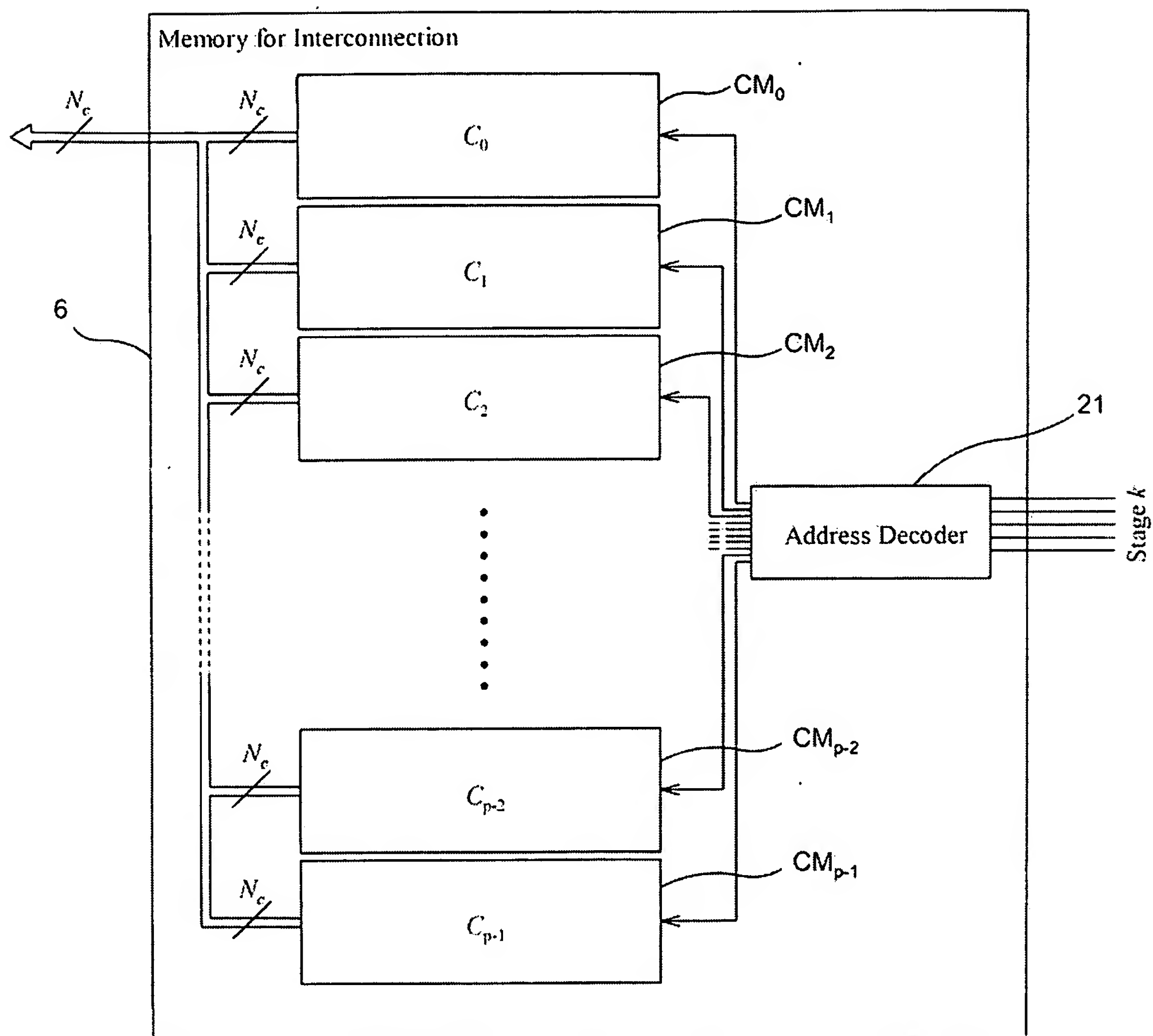


FIG. 4



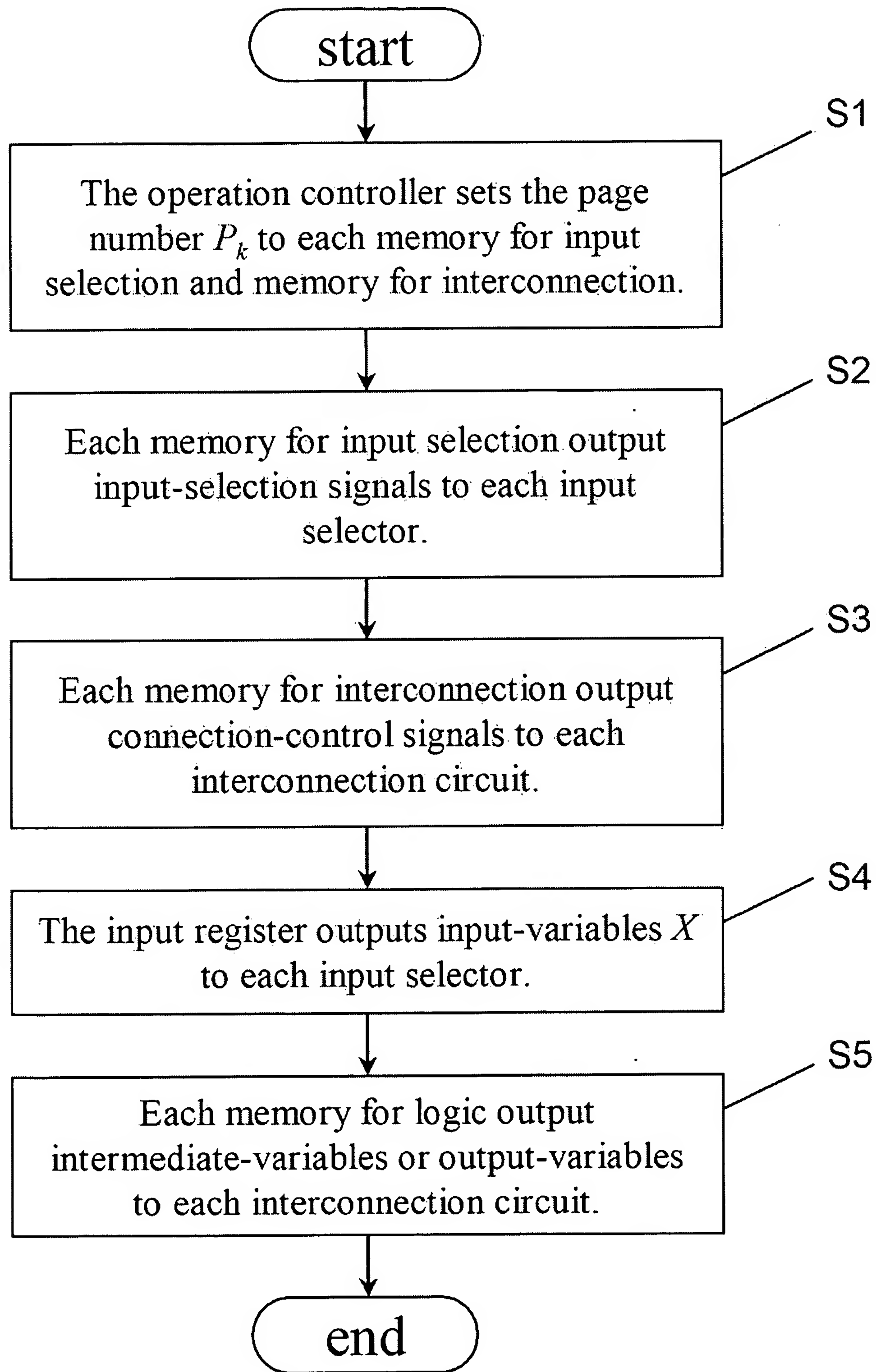
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FIG. 5



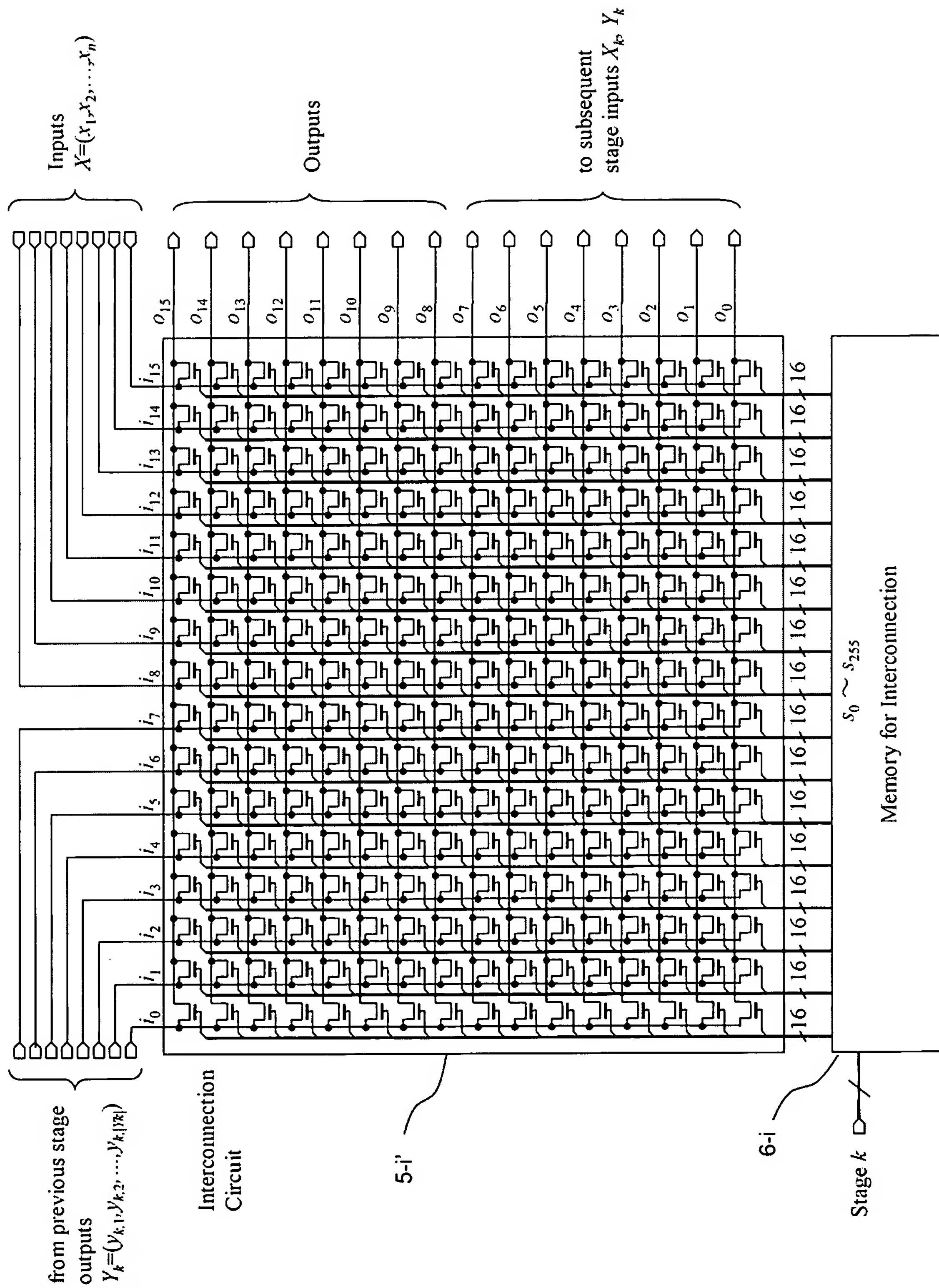
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FIG. 6



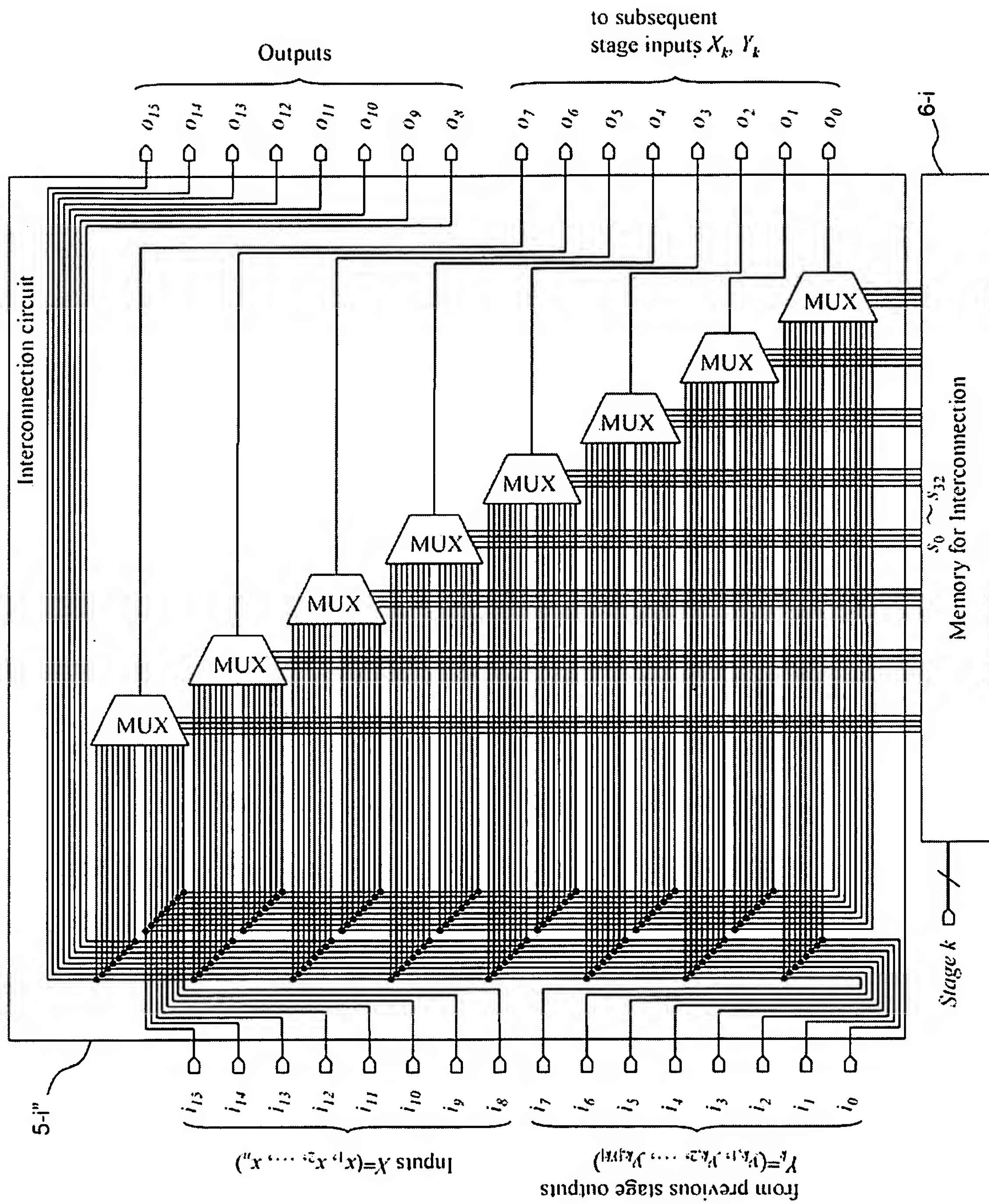
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FIG. 7



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FIG. 8



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FIG. 9

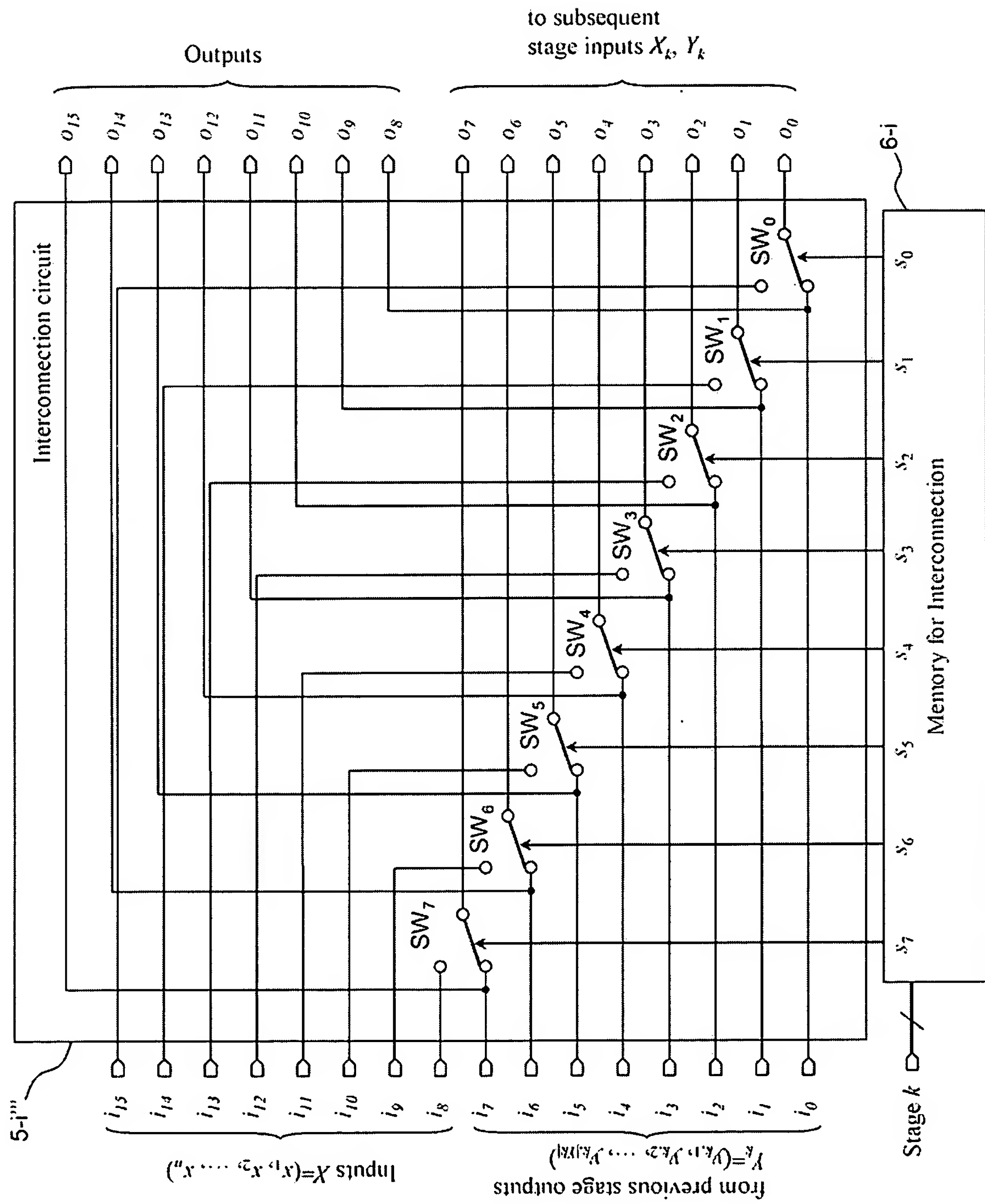
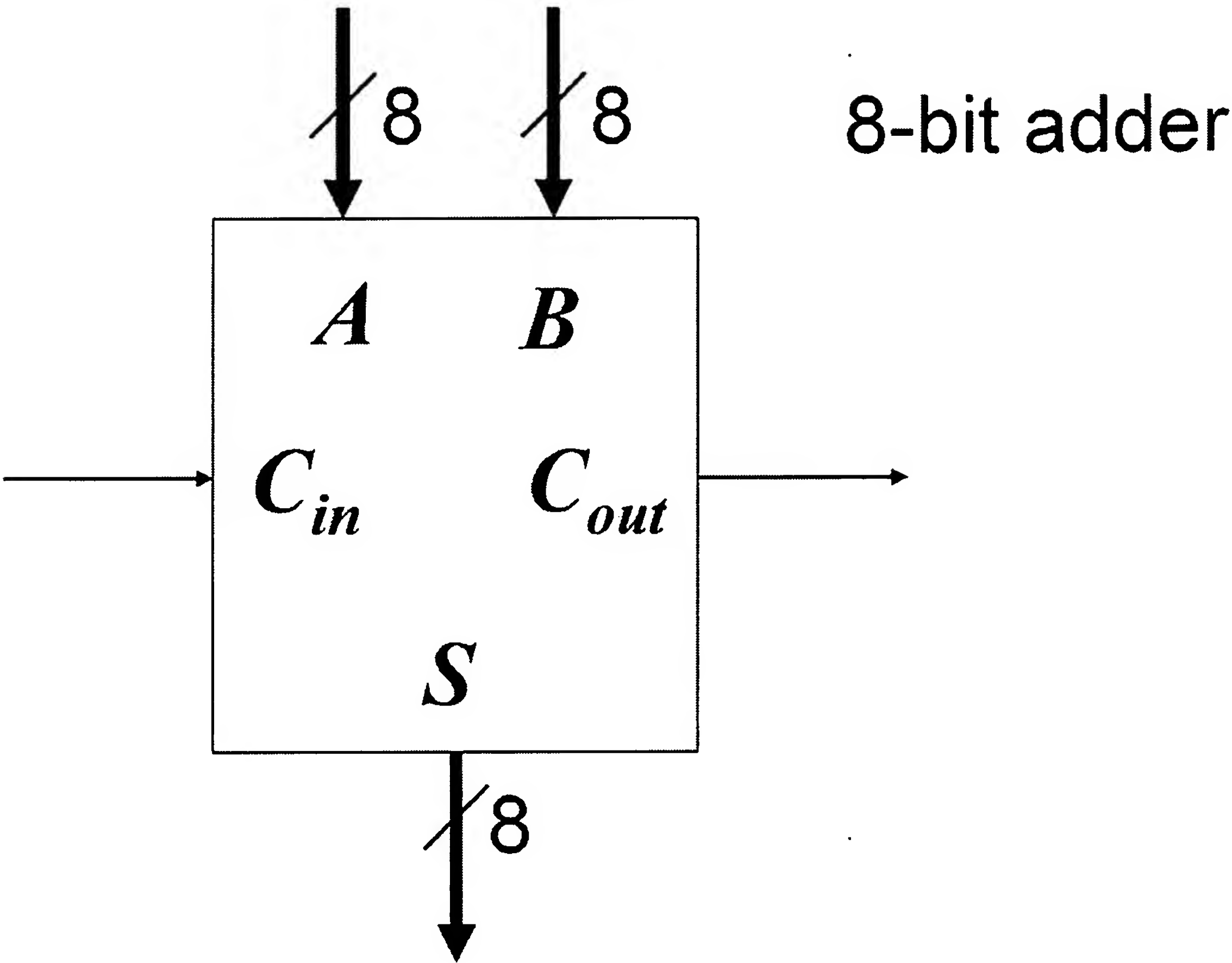
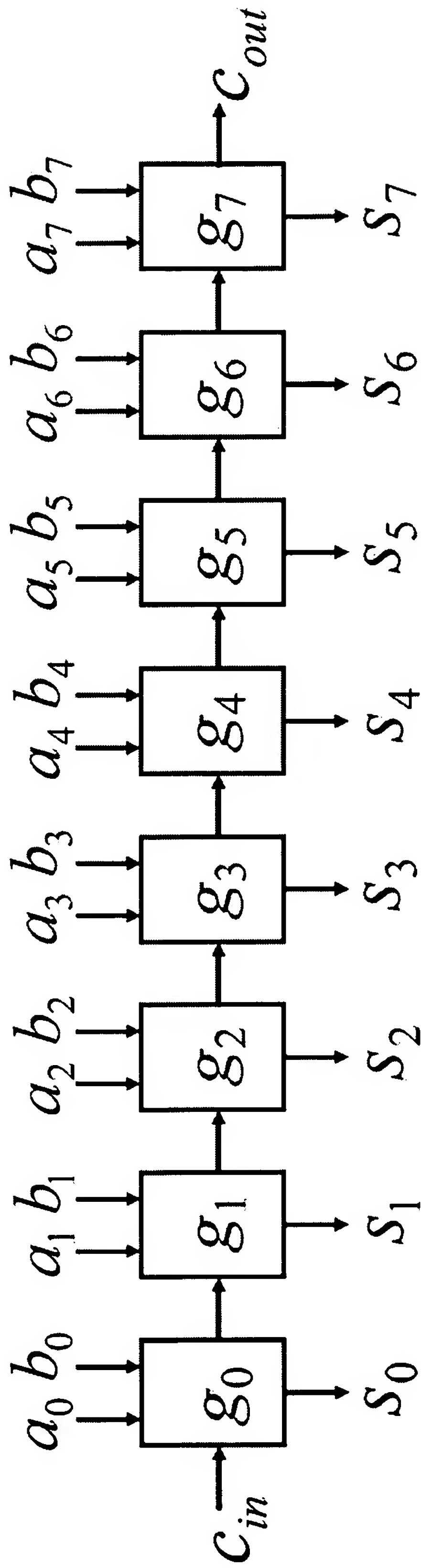


FIG. 10



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FIG. 11



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FIG. 12

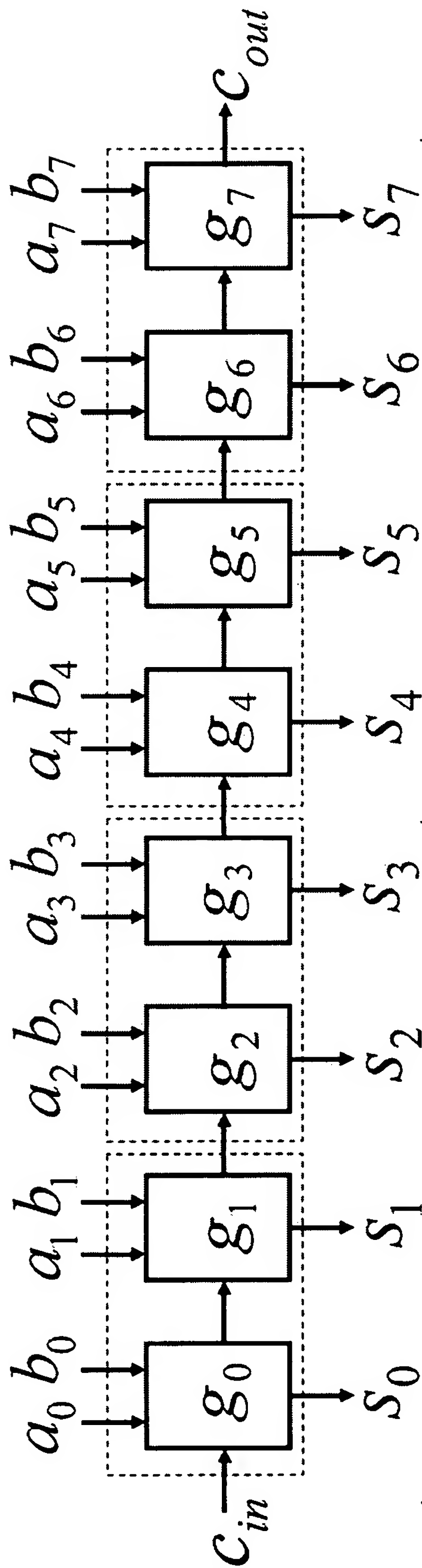


FIG. 13

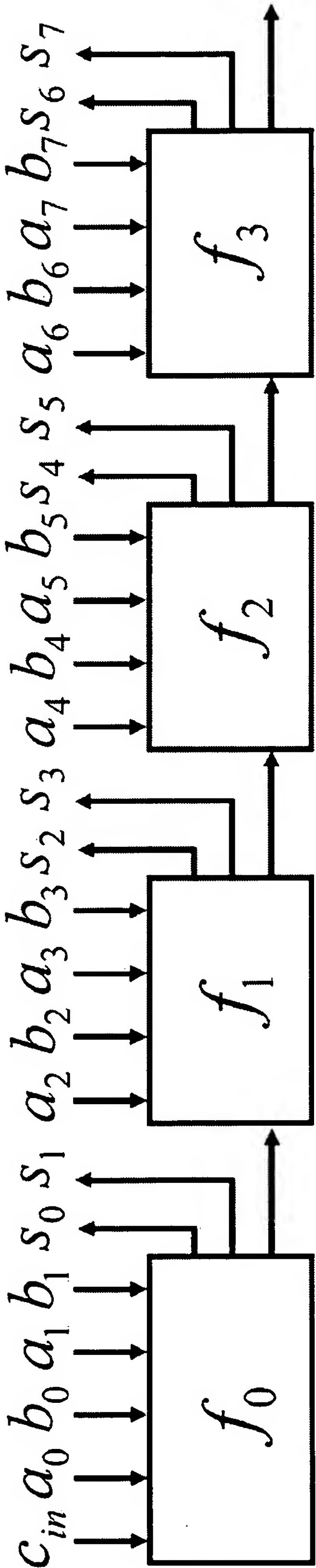


FIG. 14

c_{in}	a_1	a_0	b_1	b_0	c_{out}	s_1	s_0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	0	1	1	0	1
0	1	0	1	0	0	1	0
0	1	0	1	1	1	0	1
0	1	0	1	1	1	1	0
0	1	1	0	0	0	0	0
0	1	1	0	0	1	0	1
0	1	1	0	1	0	0	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	0	1
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1

c_{in}	a_1	a_0	b_1	b_0	c_{out}	s_1	s_0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	1
1	1	0	1	1	1	1	0
1	1	1	0	0	1	0	0
1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

FIG. 15

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	0	0	0	0	-	-	-	-	-	-	0	0	0	-	-
0	0	0	0	1	-	-	-	-	-	-	0	0	1	-	-
0	0	0	1	0	-	-	-	-	-	-	0	1	0	-	-
0	0	0	1	1	-	-	-	-	-	-	0	1	1	-	-
0	0	1	0	0	-	-	-	-	-	-	0	0	1	-	-
0	0	1	0	1	-	-	-	-	-	-	0	1	0	-	-
0	0	1	1	0	-	-	-	-	-	-	0	1	1	-	-
0	0	1	1	1	-	-	-	-	-	-	1	0	0	-	-
0	1	0	0	0	-	-	-	-	-	-	0	1	0	-	-
0	1	0	0	1	-	-	-	-	-	-	0	1	1	-	-
0	1	0	1	0	-	-	-	-	-	-	1	0	0	-	-
0	1	0	1	1	-	-	-	-	-	-	1	0	1	-	-
0	1	1	0	0	-	-	-	-	-	-	0	1	1	-	-
0	1	1	0	1	-	-	-	-	-	-	1	0	0	-	-
0	1	1	1	0	-	-	-	-	-	-	1	0	1	-	-
0	1	1	1	1	-	-	-	-	-	-	1	1	0	-	-

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
1	0	0	0	0	-	-	-	-	-	-	0	0	1	-	-
1	0	0	0	1	-	-	-	-	-	-	0	1	0	-	-
1	0	0	1	0	-	-	-	-	-	-	0	1	1	-	-
1	0	0	1	1	-	-	-	-	-	-	1	0	0	-	-
1	0	1	0	0	-	-	-	-	-	-	0	1	0	-	-
1	0	1	0	1	-	-	-	-	-	-	0	1	1	-	-
1	0	1	1	0	-	-	-	-	-	-	1	0	0	-	-
1	0	1	1	1	-	-	-	-	-	-	1	0	1	-	-
1	1	0	0	0	-	-	-	-	-	-	0	1	1	-	-
1	1	0	0	1	-	-	-	-	-	-	1	0	0	-	-
1	1	0	1	0	-	-	-	-	-	-	1	0	1	-	-
1	1	0	1	1	-	-	-	-	-	-	1	1	0	-	-
1	1	1	0	0	-	-	-	-	-	-	1	0	0	-	-
1	1	1	0	1	-	-	-	-	-	-	1	0	1	-	-
1	1	1	1	0	-	-	-	-	-	-	1	1	0	-	-
1	1	1	1	1	-	-	-	-	-	-	1	1	1	-	-

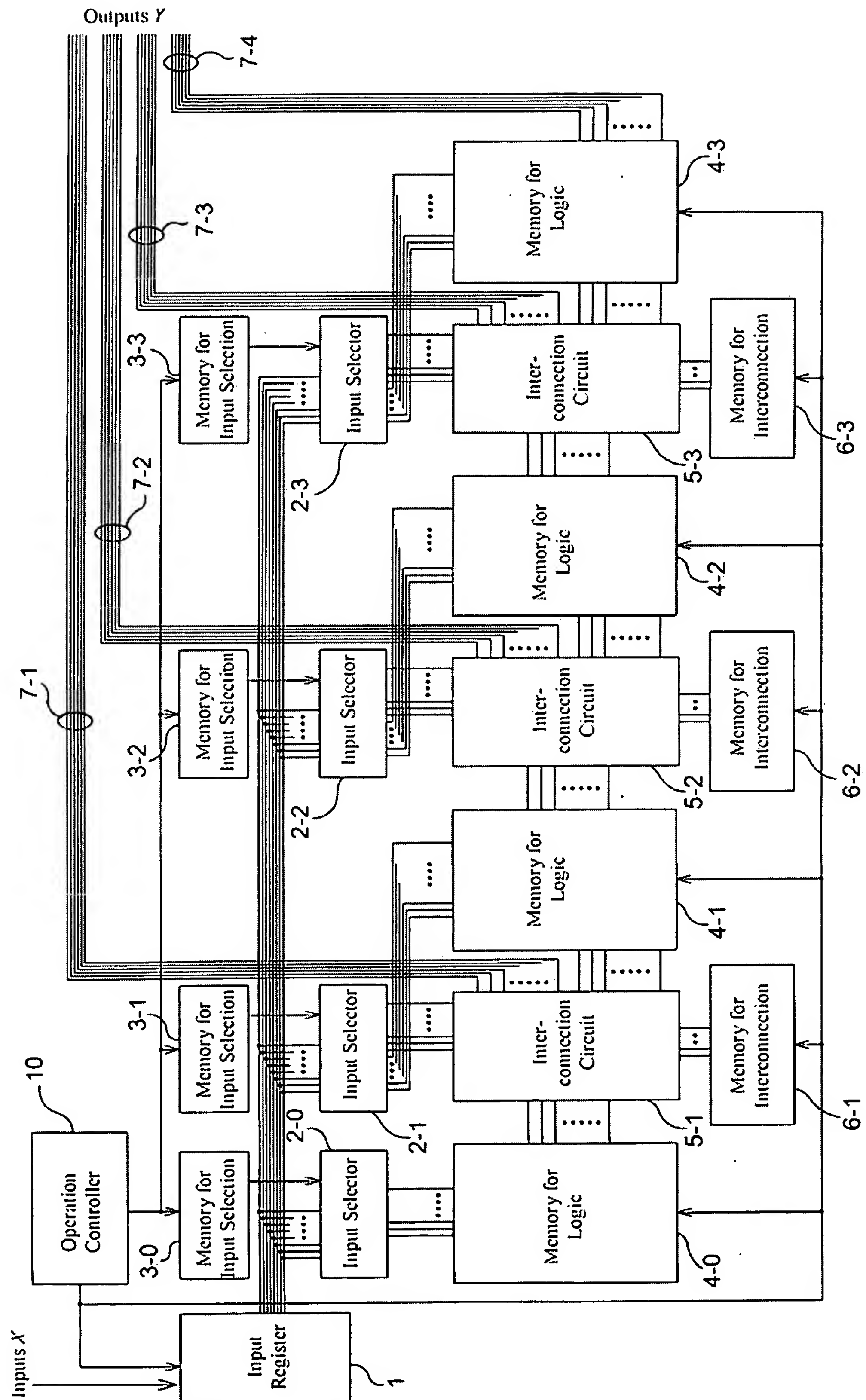
FIG. 16

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	-	-	-	0	0	0	0	-	-	-	0	0	0	-	-
0	-	-	-	0	0	0	1	-	-	-	0	0	1	-	-
0	-	-	-	0	0	1	0	-	-	-	0	1	0	-	-
0	-	-	-	0	0	1	1	-	-	-	0	1	1	-	-
0	-	-	-	0	1	0	0	-	-	-	0	0	1	-	-
0	-	-	-	0	1	0	1	-	-	-	0	1	0	-	-
0	-	-	-	0	1	1	0	-	-	-	0	1	1	-	-
0	-	-	-	0	1	1	1	-	-	-	1	0	0	-	-
0	-	-	-	1	0	0	0	-	-	-	0	1	0	-	-
0	-	-	-	1	0	0	1	-	-	-	0	1	1	-	-
0	-	-	-	1	0	1	0	-	-	-	1	0	0	-	-
0	-	-	-	1	0	1	1	-	-	-	1	0	1	-	-
0	-	-	-	1	1	0	0	-	-	-	0	1	1	-	-
0	-	-	-	1	1	0	1	-	-	-	1	0	0	-	-
0	-	-	-	1	1	1	0	-	-	-	1	0	1	-	-
0	-	-	-	1	1	1	1	-	-	-	1	1	0	-	-

Address								Memory value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
1	-	-	-	0	0	0	0	-	-	-	0	0	1	-	-
1	-	-	-	0	0	0	1	-	-	-	0	1	0	-	-
1	-	-	-	0	0	1	0	-	-	-	0	1	1	-	-
1	-	-	-	0	0	1	1	-	-	-	1	0	0	-	-
1	-	-	-	0	1	0	0	-	-	-	0	1	0	-	-
1	-	-	-	0	1	0	1	-	-	-	0	1	1	-	-
1	-	-	-	0	1	1	0	-	-	-	1	0	0	-	-
1	-	-	-	0	1	1	1	-	-	-	1	0	1	-	-
1	-	-	-	1	0	0	0	-	-	-	0	1	1	-	-
1	-	-	-	1	0	0	1	-	-	-	1	0	0	-	-
1	-	-	-	1	0	1	0	-	-	-	1	0	1	-	-
1	-	-	-	1	0	1	1	-	-	-	1	1	0	-	-
1	-	-	-	1	1	0	0	-	-	-	1	0	0	-	-
1	-	-	-	1	1	0	1	-	-	-	1	0	1	-	-
1	-	-	-	1	1	1	0	-	-	-	1	1	0	-	-
1	-	-	-	1	1	1	1	-	-	-	1	1	1	-	-

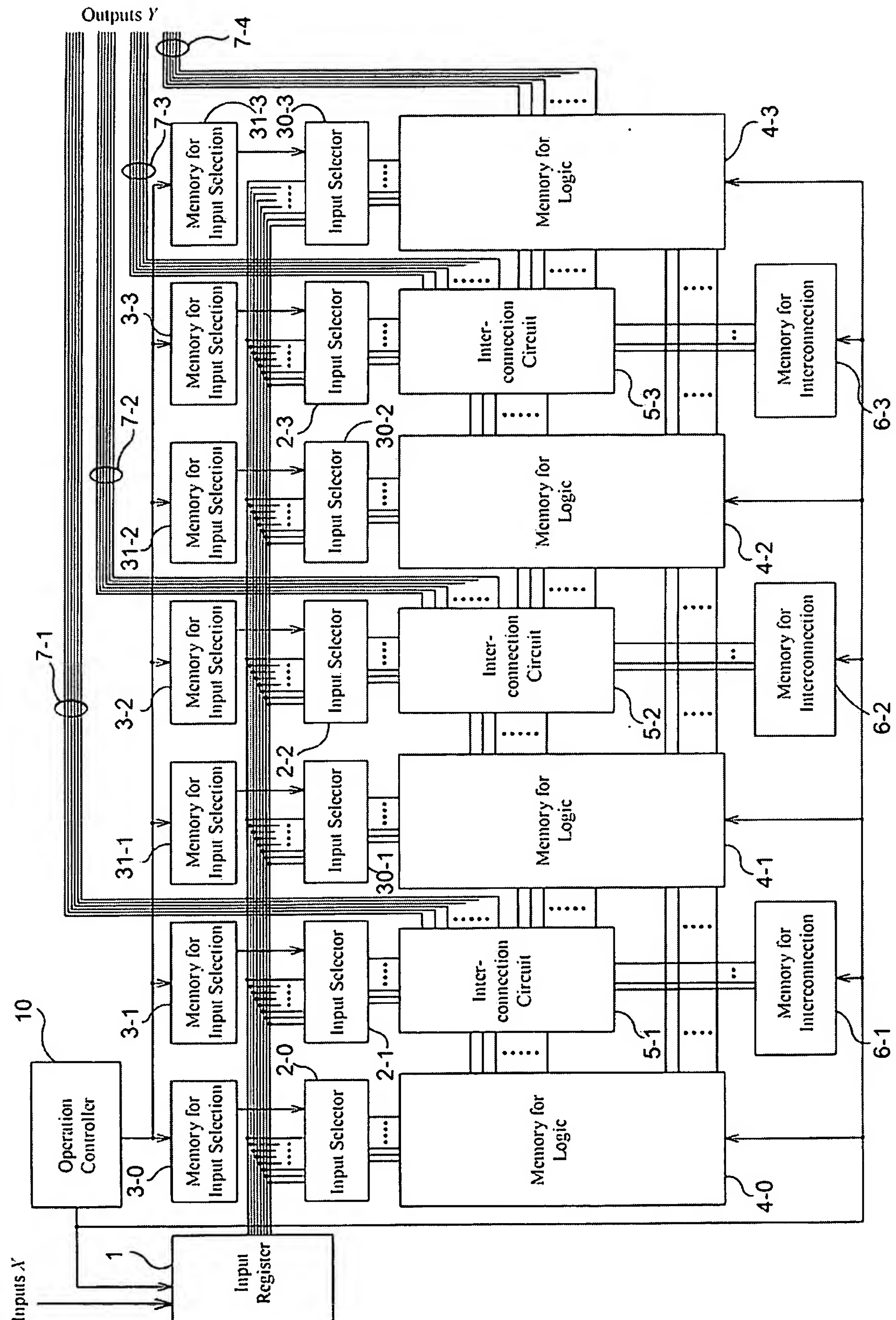
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FIG. 17



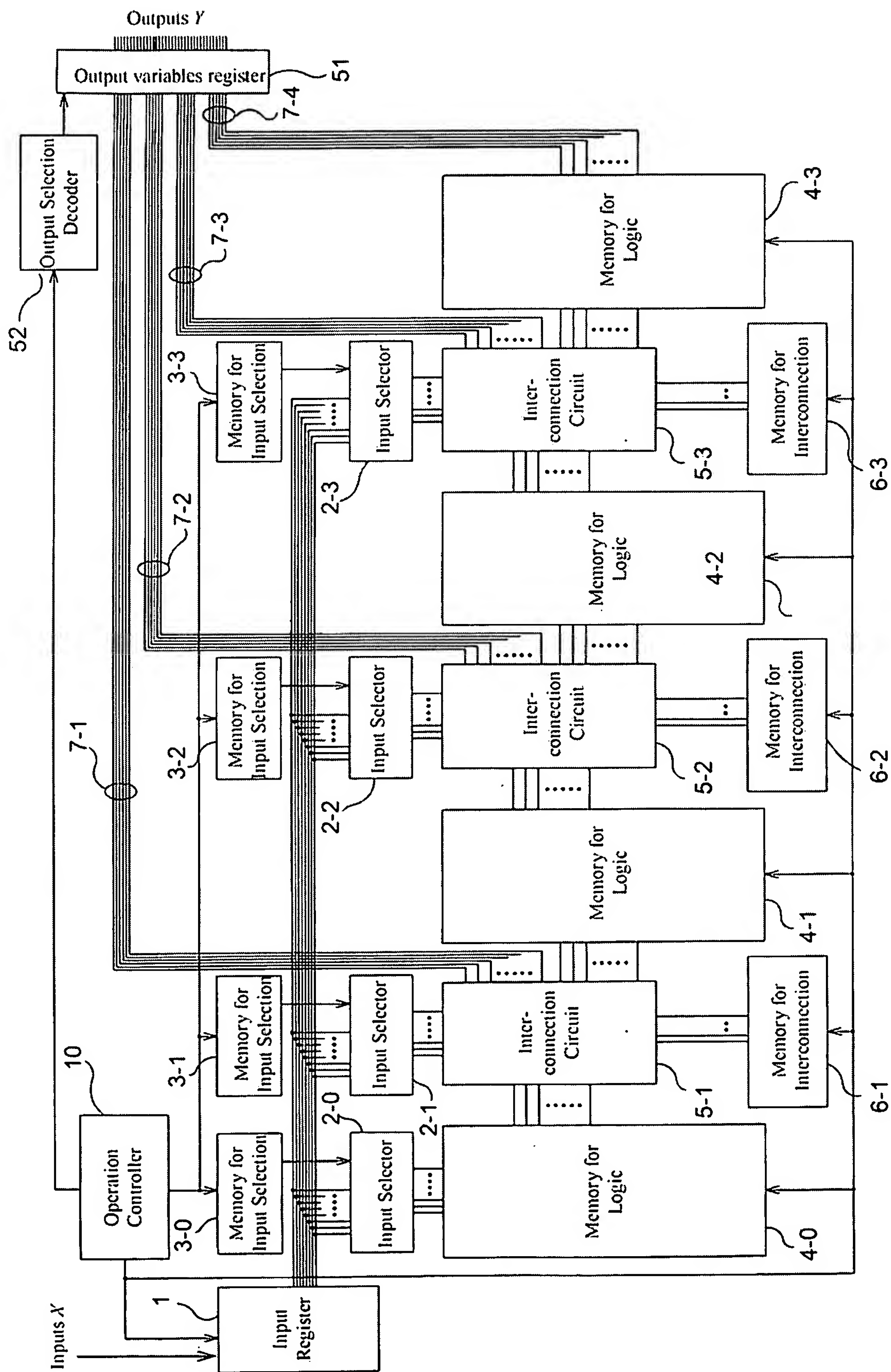
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FIG. 18



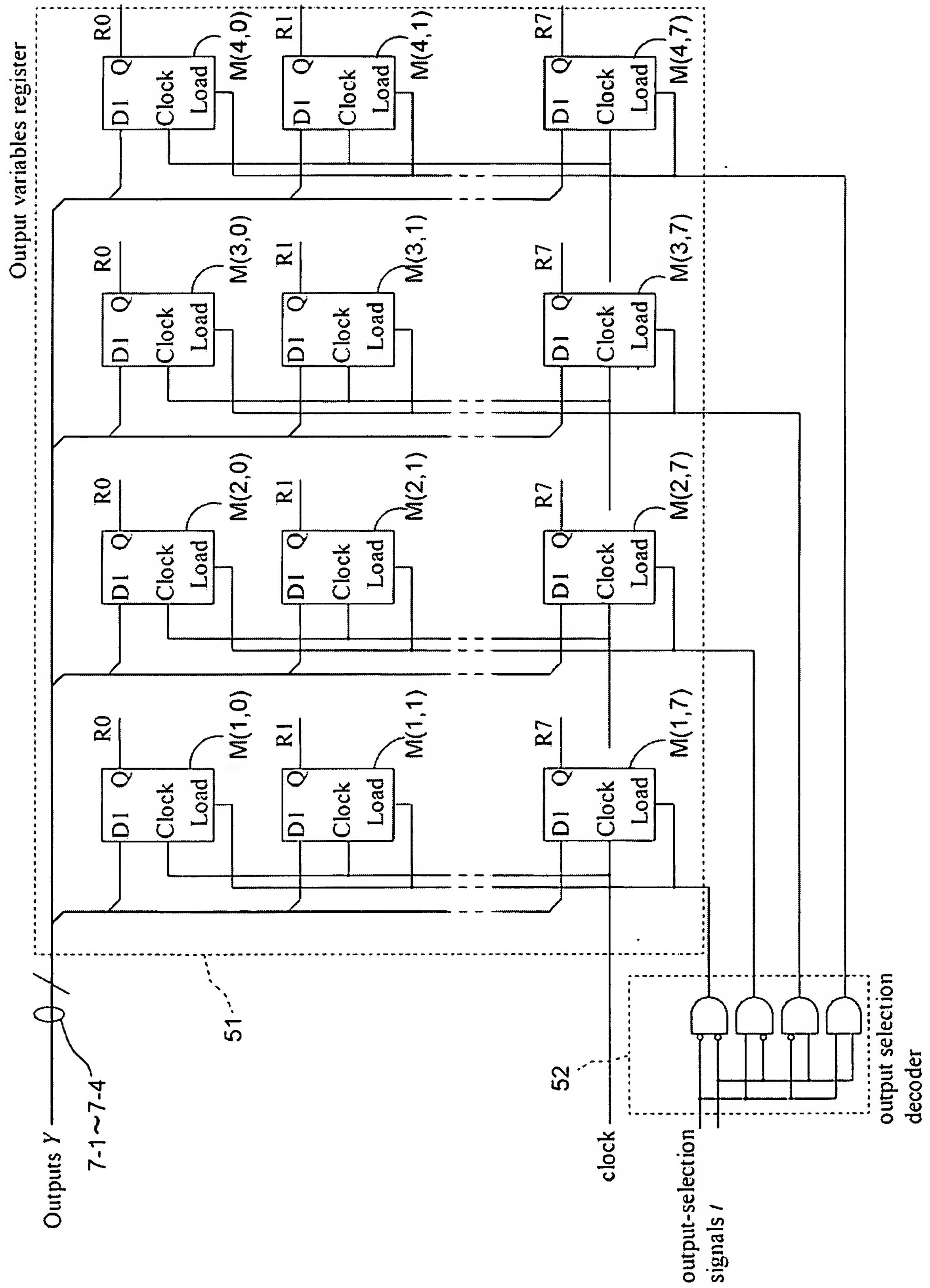
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FIG. 19



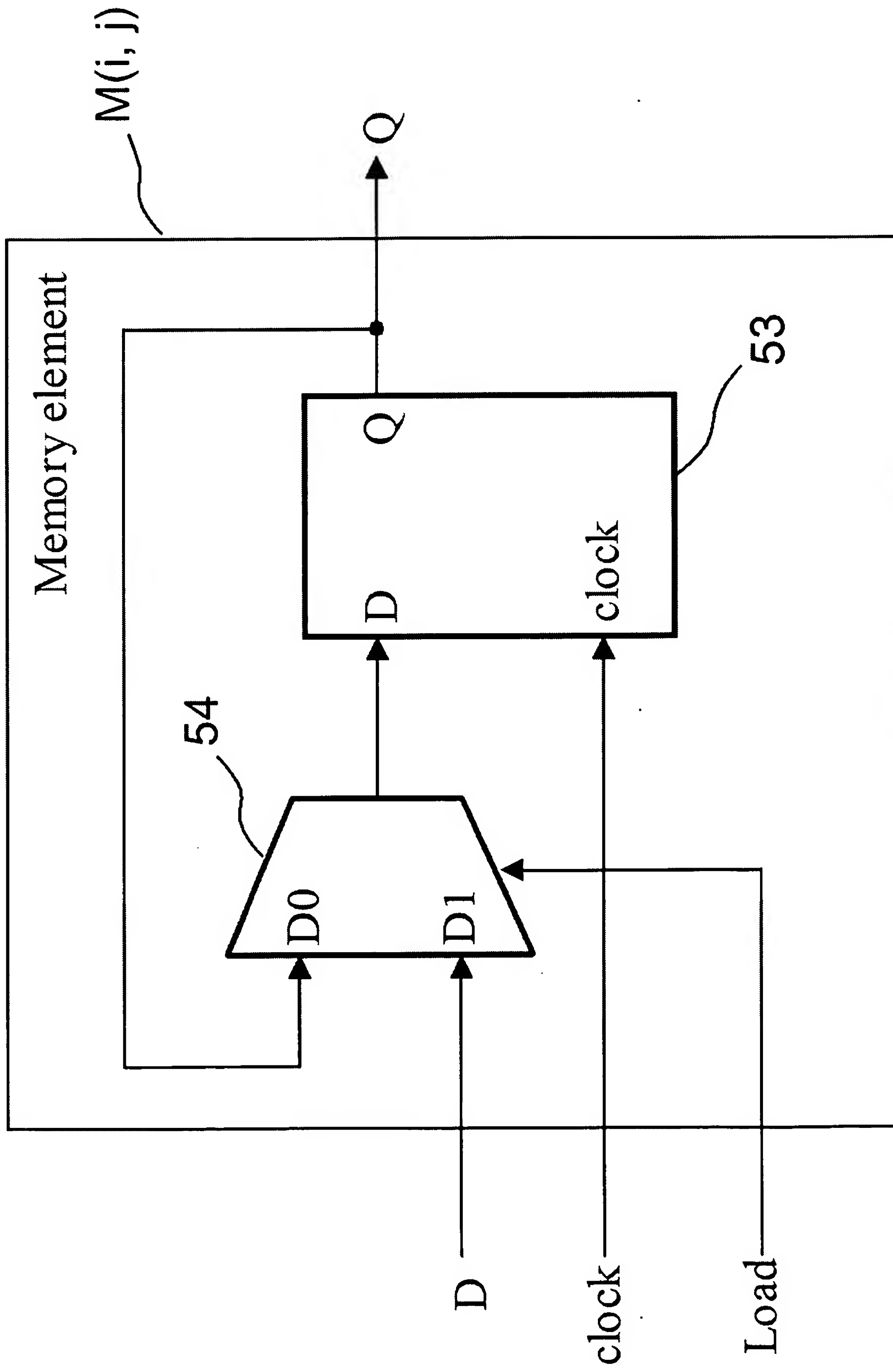
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FIG. 20



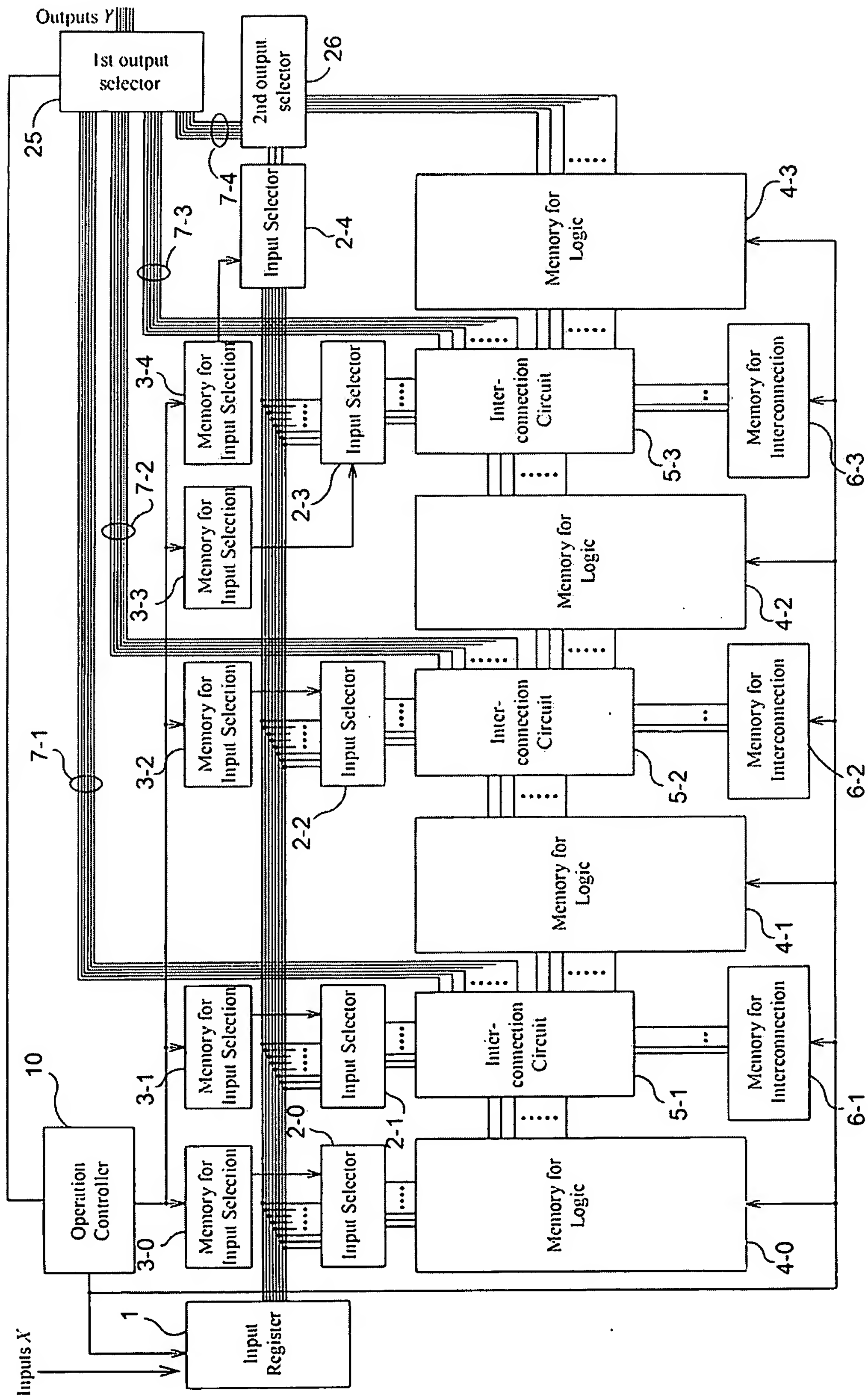
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FIG. 21



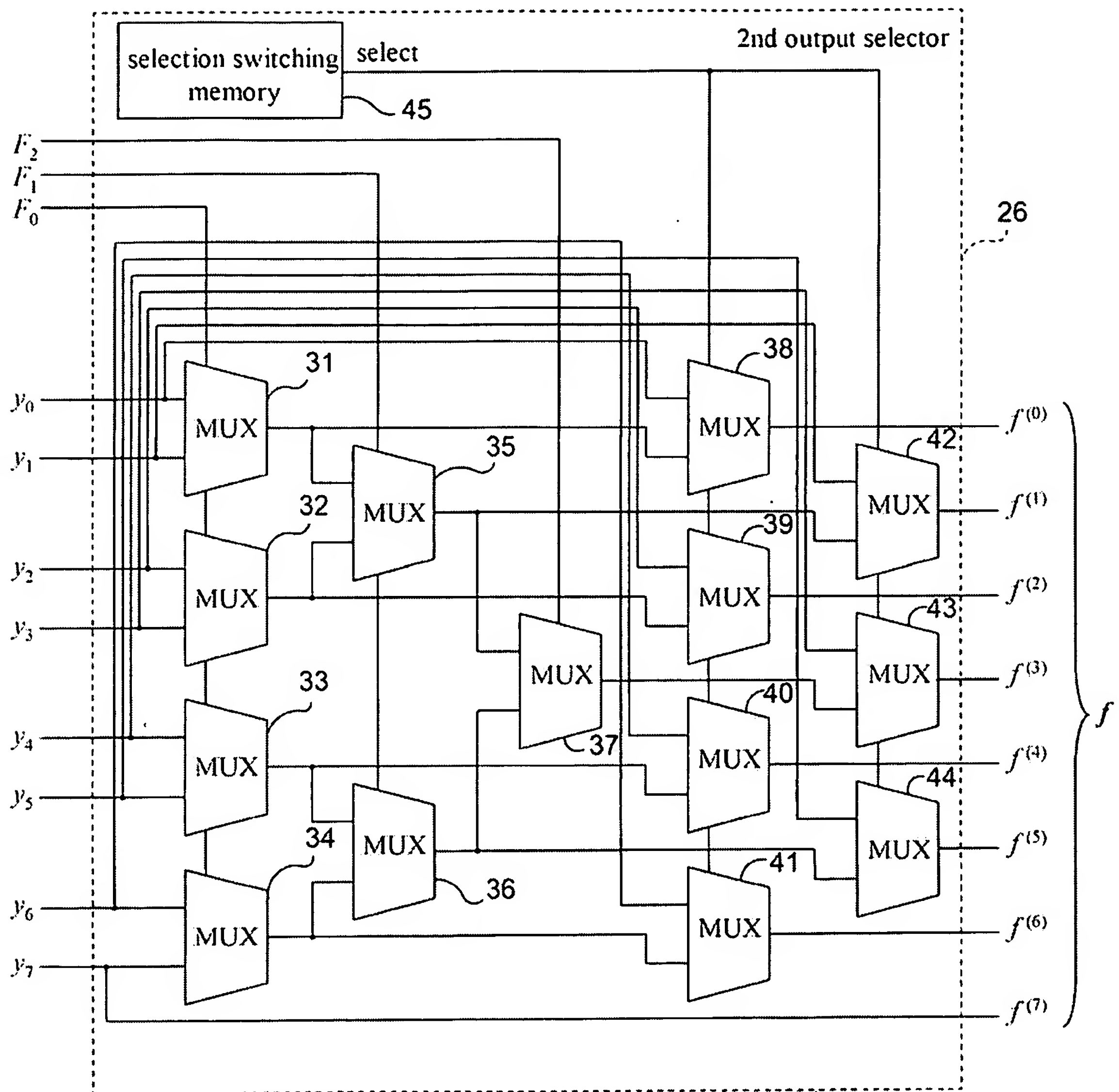
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FIG. 22



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FIG. 23



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FIG. 24

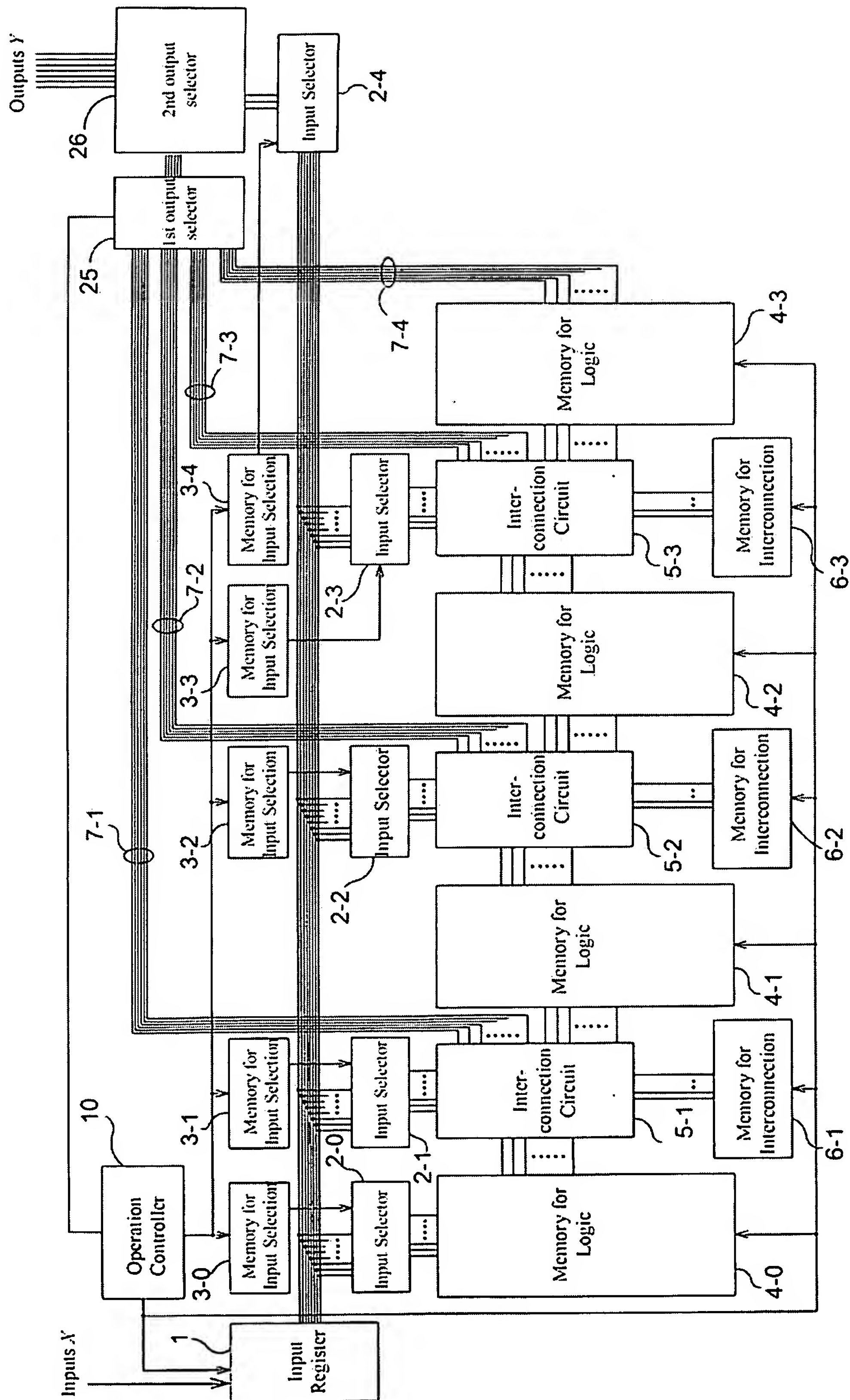


FIG. 25

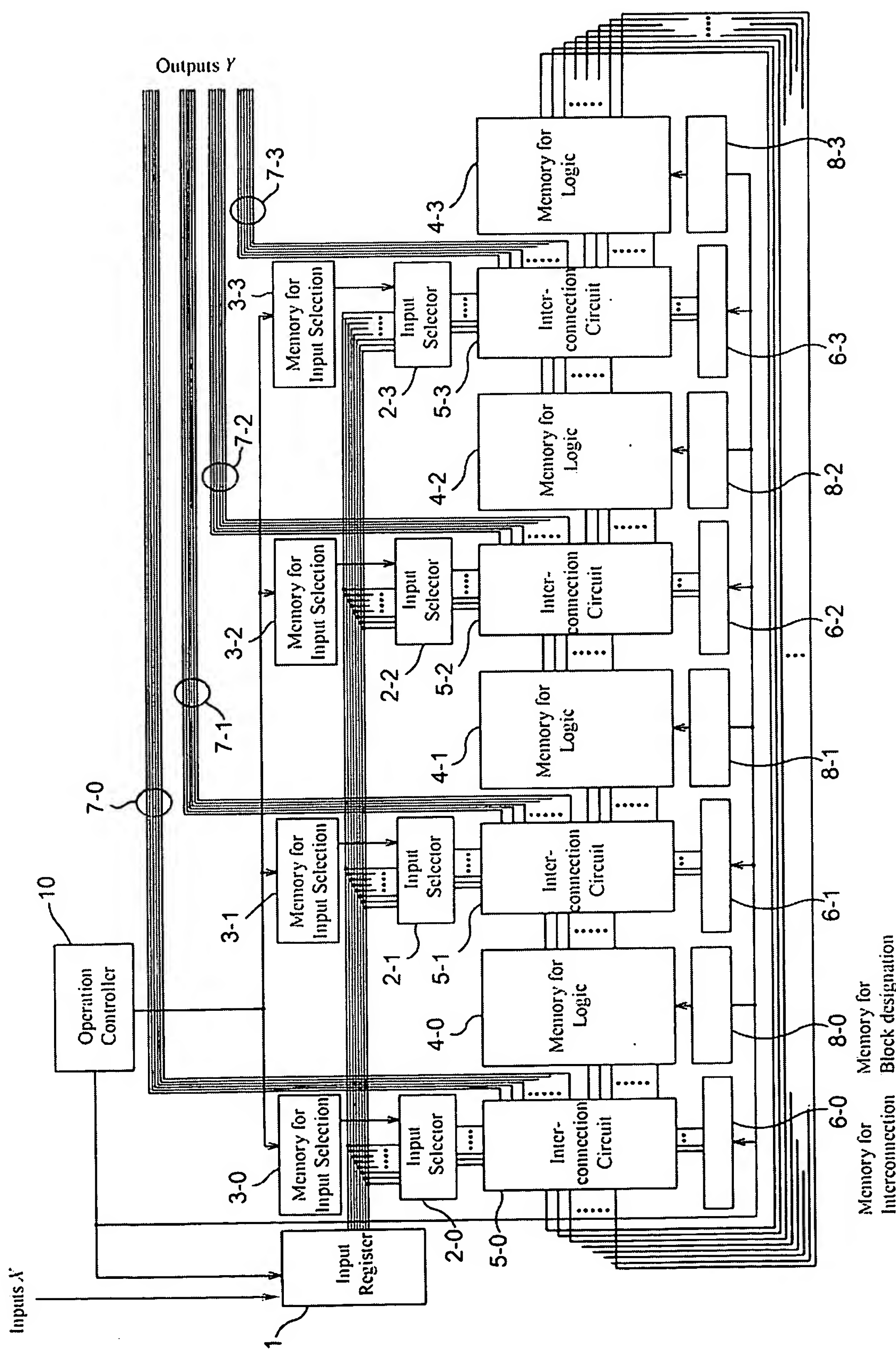
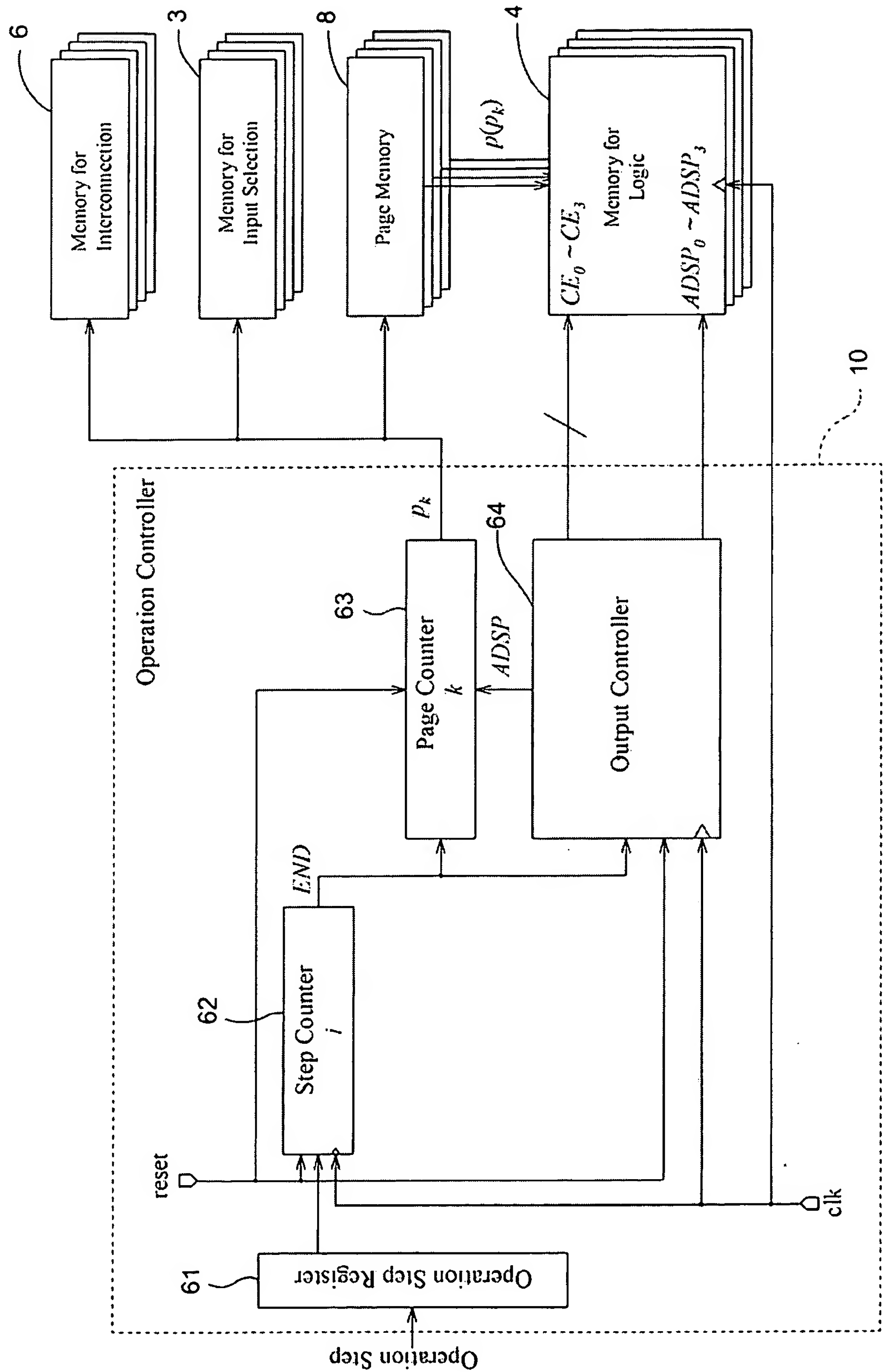
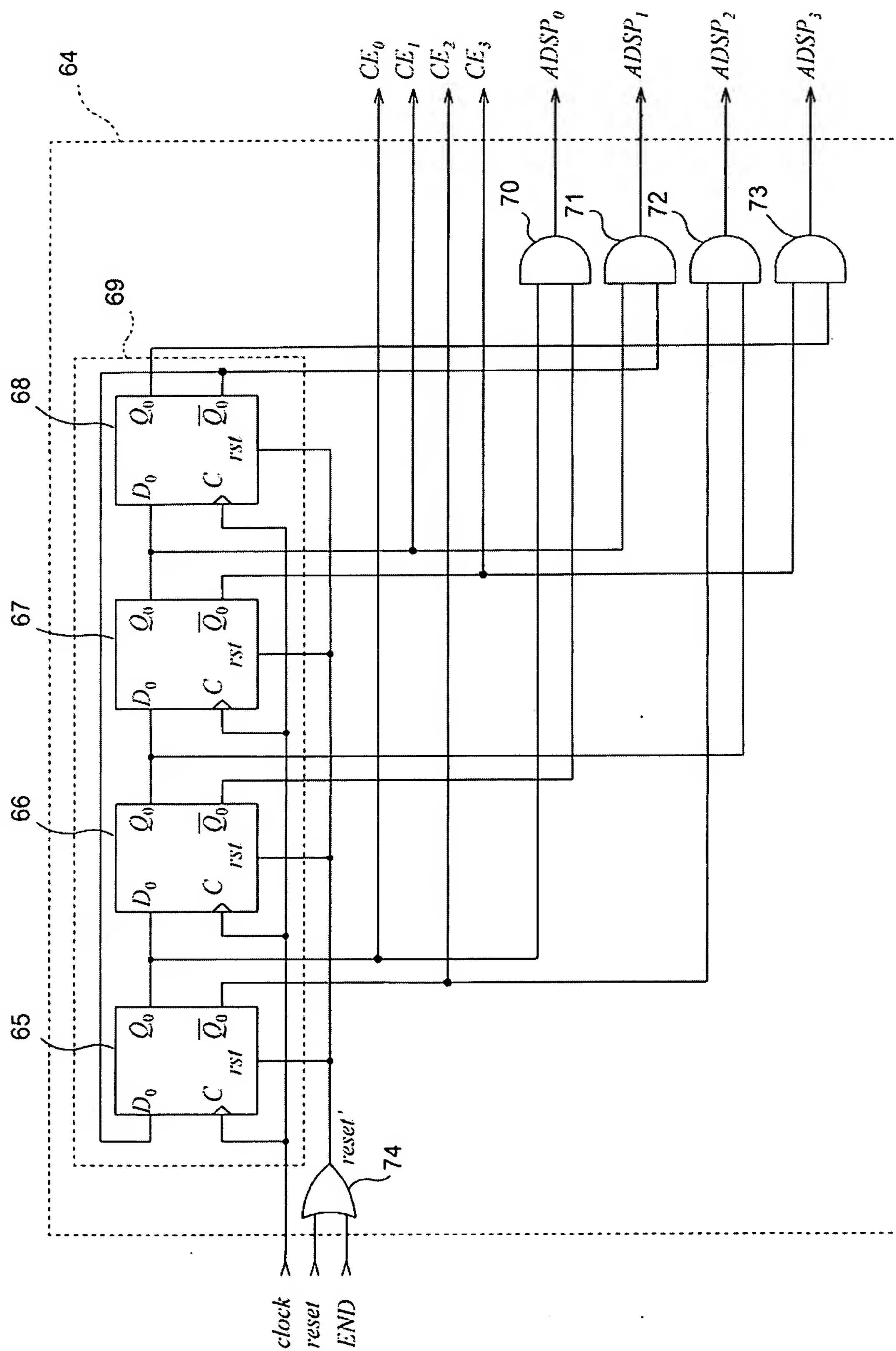


FIG. 26



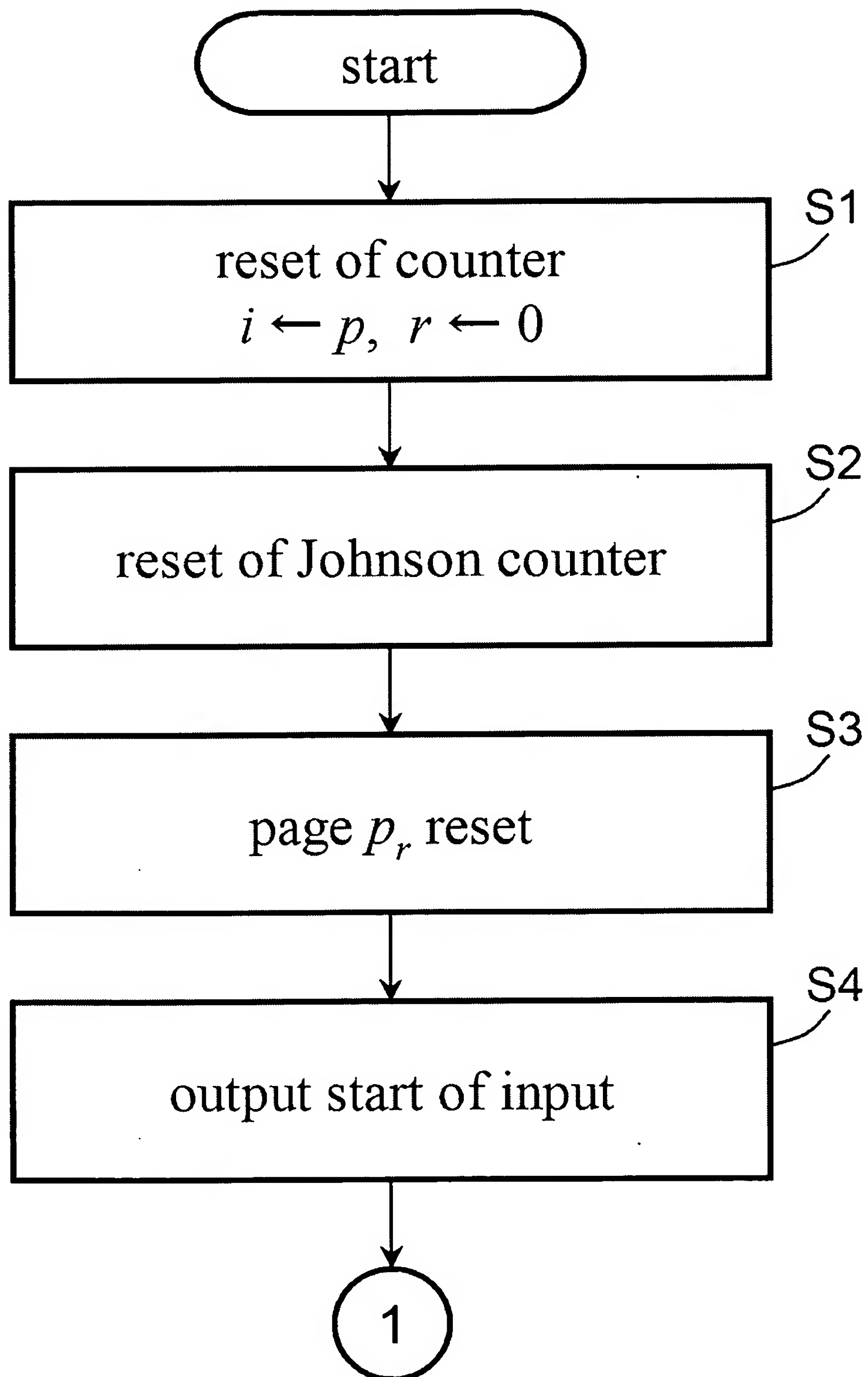
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FIG. 27



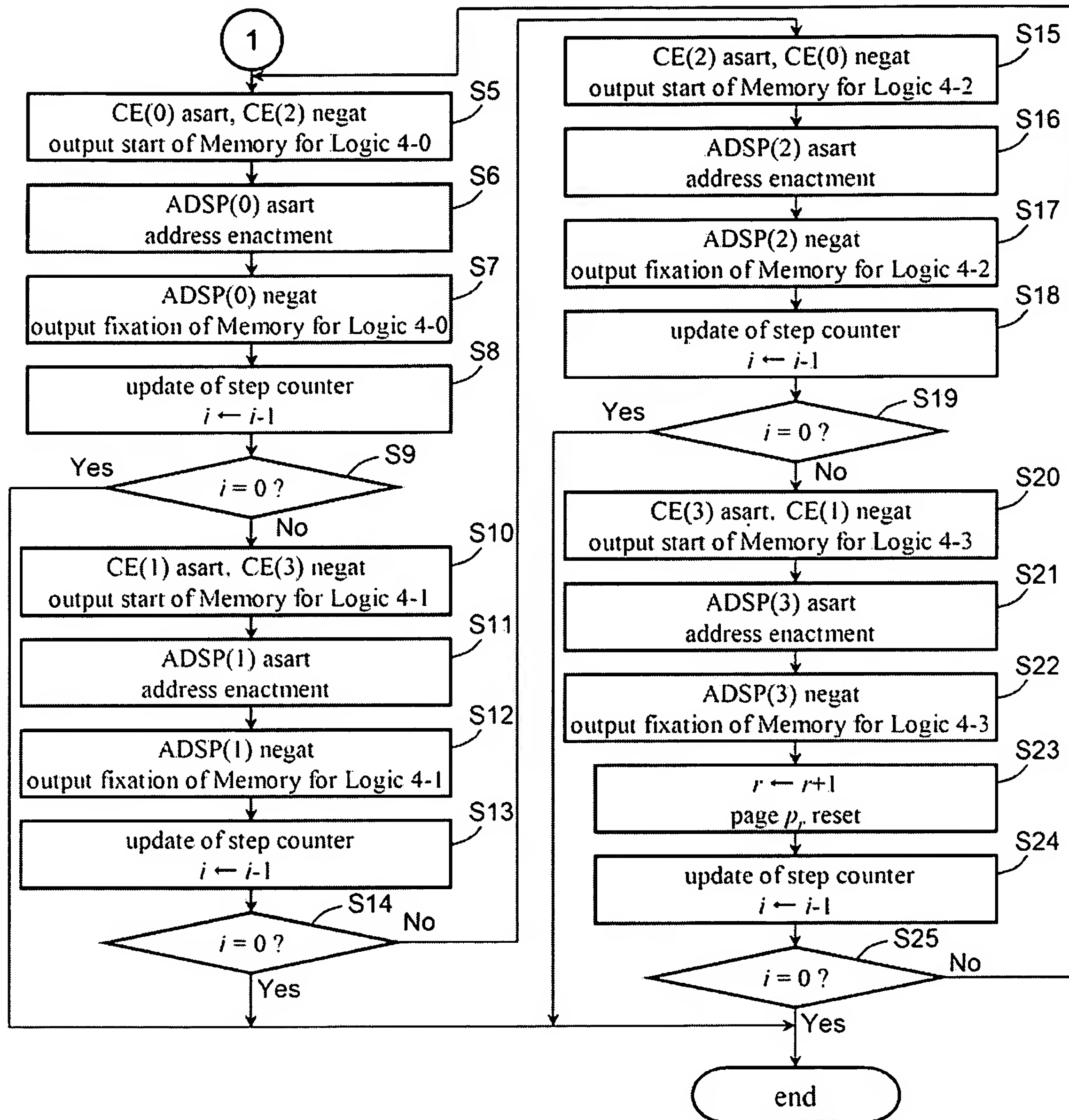
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FIG. 28a



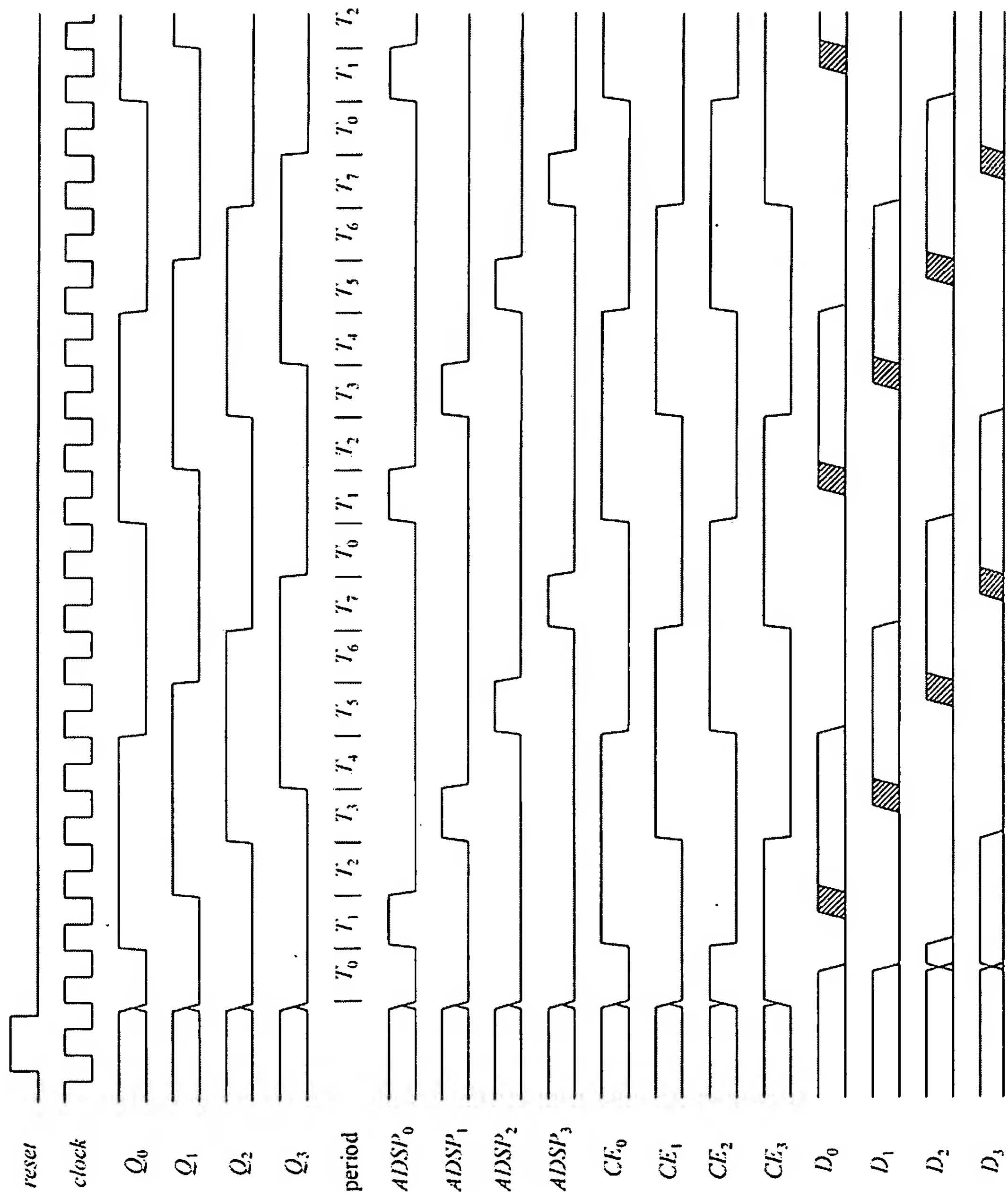
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FIG. 28b



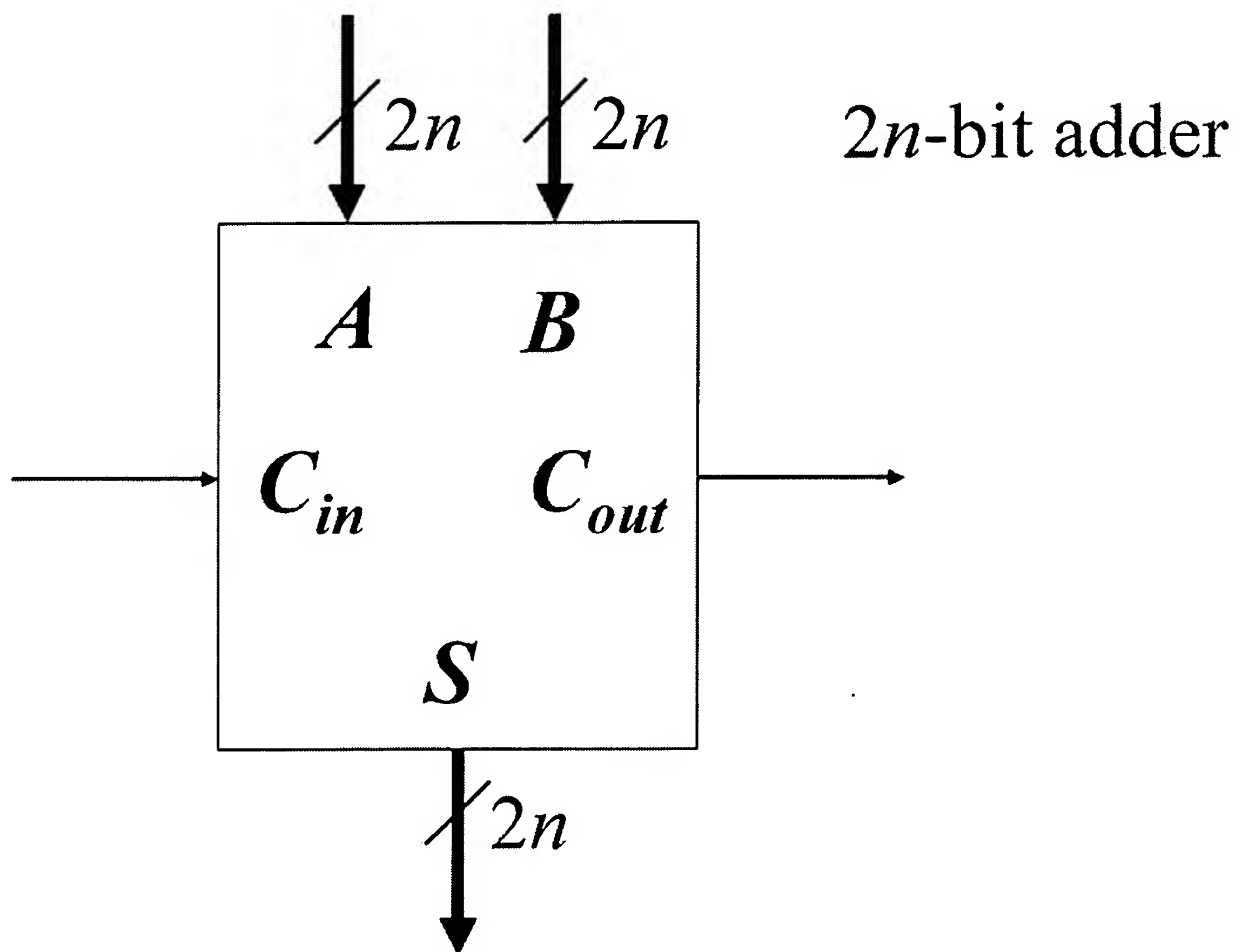
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FIG. 29



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FIG. 30



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FIG. 31

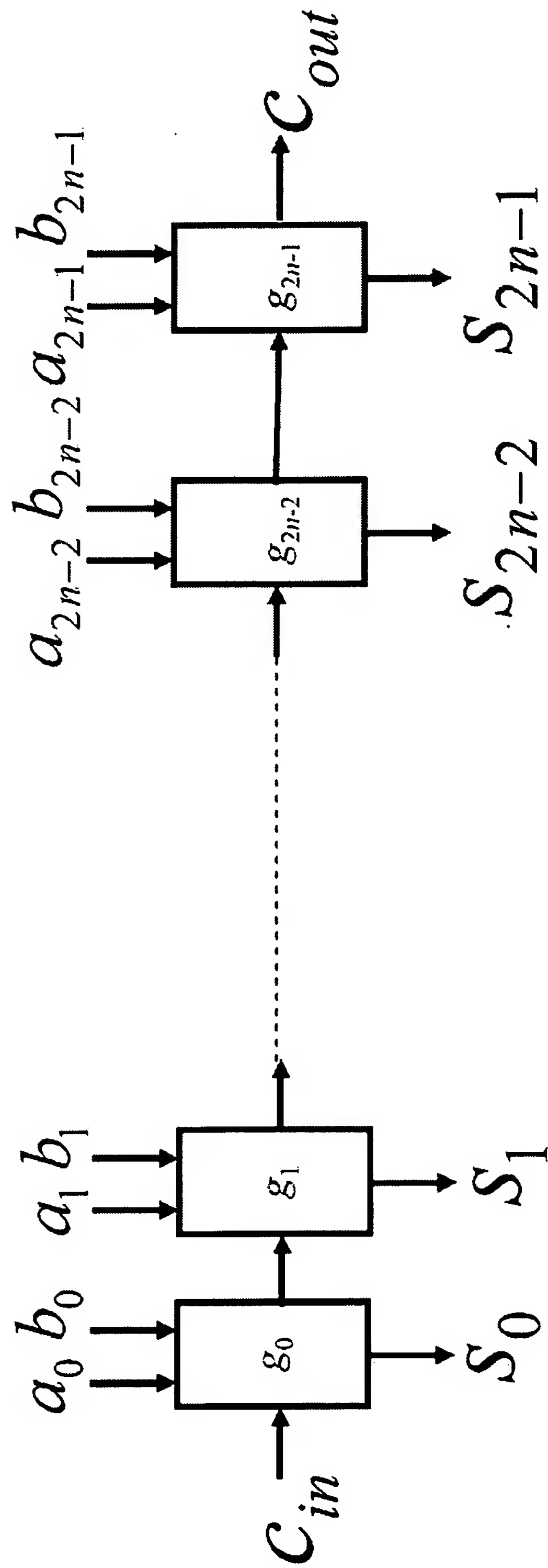
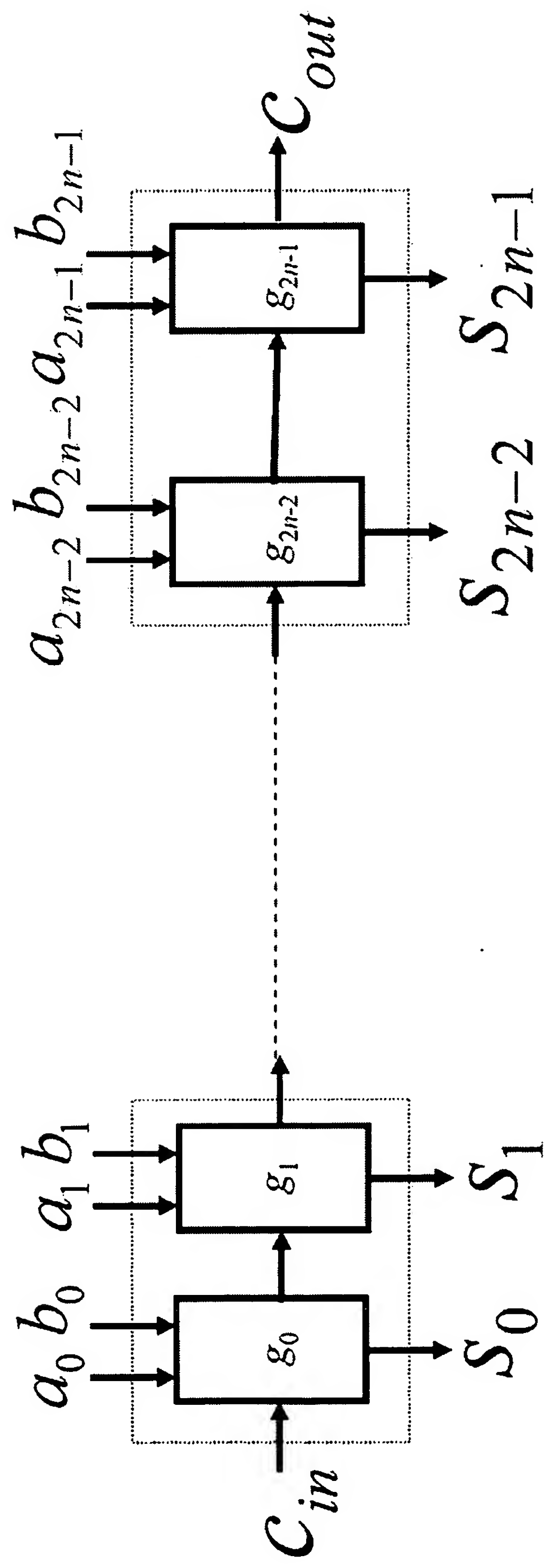


FIG. 32



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FIG. 33

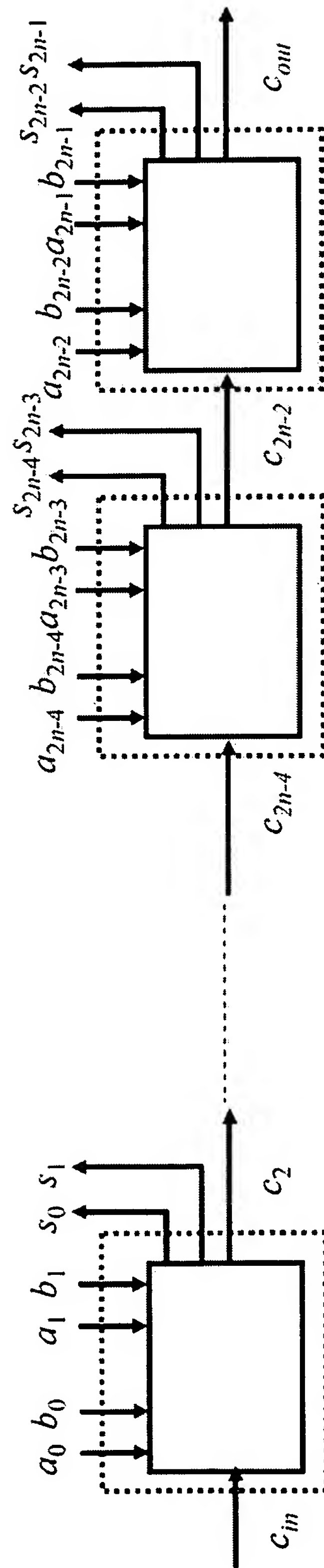


FIG. 34

C_{in}	a_1	a_0	b_1	b_0	C_{out}	s_1	s_0
0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	1
0	0	0	1	0	0	1	0
0	0	0	1	1	0	1	1
0	0	1	0	0	0	0	1
0	0	1	0	1	0	1	0
0	0	1	1	0	0	1	1
0	0	1	1	1	1	0	0
0	1	0	0	0	0	1	0
0	1	0	0	1	0	1	1
0	1	0	1	0	1	0	0
0	1	0	1	1	1	0	1
0	1	1	0	0	1	0	1
0	1	1	0	1	1	0	0
0	1	1	1	0	1	1	0
0	1	1	1	1	1	0	1
0	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1

C_{in}	a_1	a_0	b_1	b_0	C_{out}	s_1	s_0
1	0	0	0	0	0	0	1
1	0	0	0	1	0	1	0
1	0	0	1	0	0	1	1
1	0	0	1	1	1	0	0
1	0	1	0	0	0	1	0
1	0	1	0	1	0	1	1
1	0	1	1	0	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	0	1	1
1	1	0	0	1	1	0	0
1	1	0	1	0	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	0	1	1	0
1	1	1	0	1	1	0	1
1	1	1	1	0	1	1	0
1	1	1	1	1	1	1	1

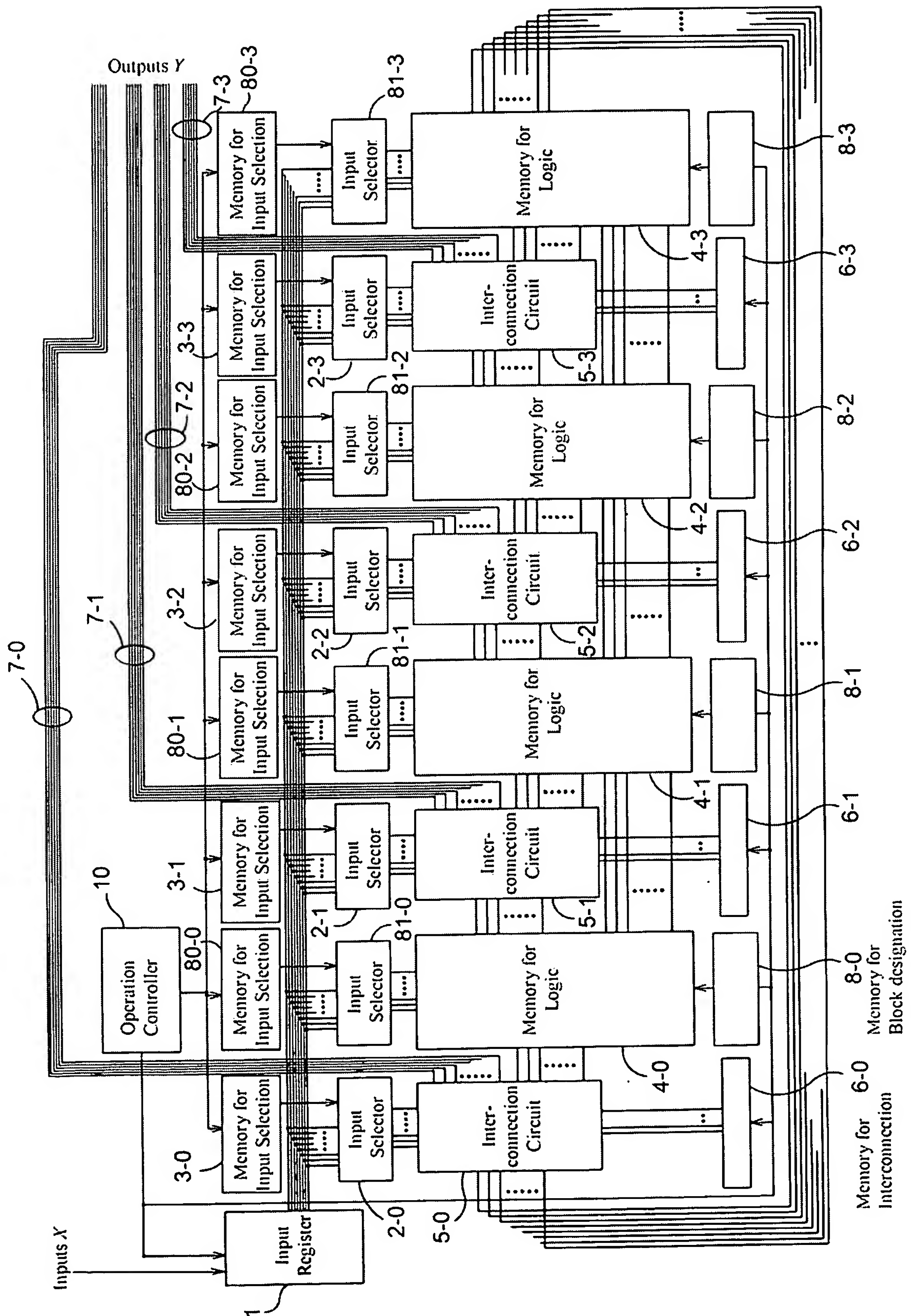
FIG. 35

address								output value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	0	0	0	0	0	0	0	-	-	-	0	0	1	-	-
0	0	0	0	1	-	-	-	-	-	-	0	1	0	-	-
0	0	0	1	0	-	-	-	-	-	-	0	1	1	-	-
0	0	0	1	1	-	-	-	-	-	-	1	0	0	-	-
0	0	1	0	0	-	-	-	-	-	-	0	1	0	-	-
0	0	1	0	1	-	-	-	-	-	-	0	1	1	-	-
0	0	1	1	0	-	-	-	-	-	-	1	0	0	-	-
0	0	1	1	1	-	-	-	-	-	-	1	0	1	-	-
0	1	0	0	0	-	-	-	-	-	-	0	1	1	-	-
0	1	0	0	1	-	-	-	-	-	-	1	0	0	-	-
0	1	0	1	0	-	-	-	-	-	-	1	0	1	-	-
0	1	0	1	1	-	-	-	-	-	-	1	0	0	-	-
0	1	1	0	0	-	-	-	-	-	-	1	0	1	-	-
0	1	1	0	1	-	-	-	-	-	-	1	1	0	-	-
0	1	1	1	0	-	-	-	-	-	-	1	1	0	-	-
0	1	1	1	1	-	-	-	-	-	-	1	1	1	-	-

FIG. 36

address								output value							
i_0	i_1	i_2	i_3	i_4	i_5	i_6	i_7	o_7	o_6	o_5	o_4	o_3	o_2	o_1	o_0
0	-	-	-	0	0	0	0	-	-	-	0	0	1	-	-
0	-	-	-	0	0	0	1	-	-	-	0	1	0	-	-
0	-	-	-	0	0	1	0	-	-	-	0	1	1	-	-
0	-	-	-	0	0	1	1	-	-	-	1	0	0	-	-
0	-	-	-	0	1	0	0	-	-	-	0	1	0	-	-
0	-	-	-	0	1	0	1	-	-	-	0	1	1	-	-
0	-	-	-	0	1	1	0	-	-	-	1	0	0	-	-
0	-	-	-	0	1	1	1	-	-	-	1	0	1	-	-
0	-	-	-	1	0	0	0	-	-	-	0	1	1	-	-
0	-	-	-	1	0	0	1	-	-	-	1	0	0	-	-
0	-	-	-	1	0	1	0	-	-	-	1	0	1	-	-
0	-	-	-	1	0	1	1	-	-	-	1	0	0	-	-
0	-	-	-	1	1	0	0	-	-	-	1	0	0	-	-
0	-	-	-	1	1	0	1	-	-	-	1	0	1	-	-
0	-	-	-	1	1	1	0	-	-	-	1	0	0	-	-
0	-	-	-	1	1	1	1	-	-	-	1	0	1	-	-

FIG. 37



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FIG. 38

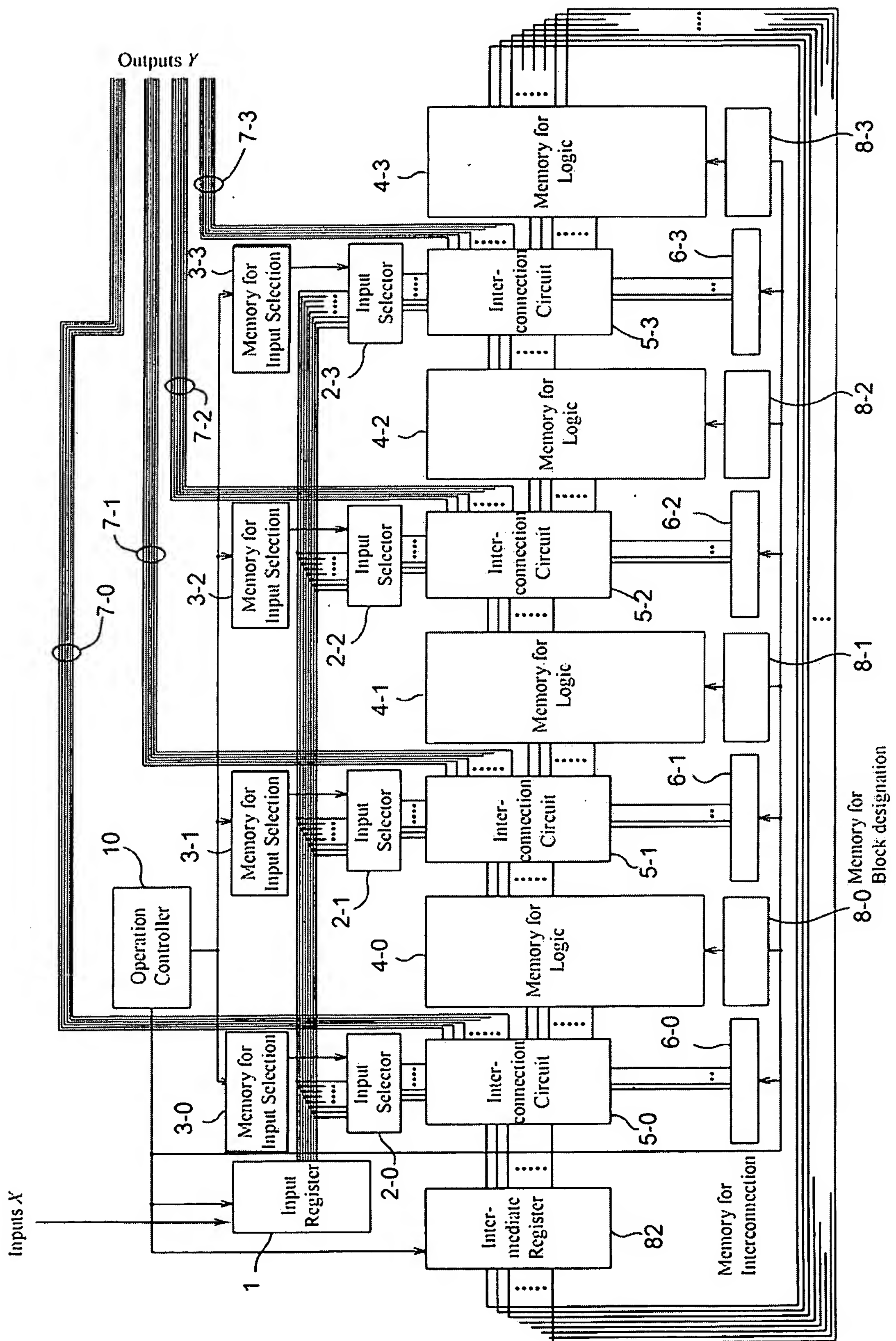
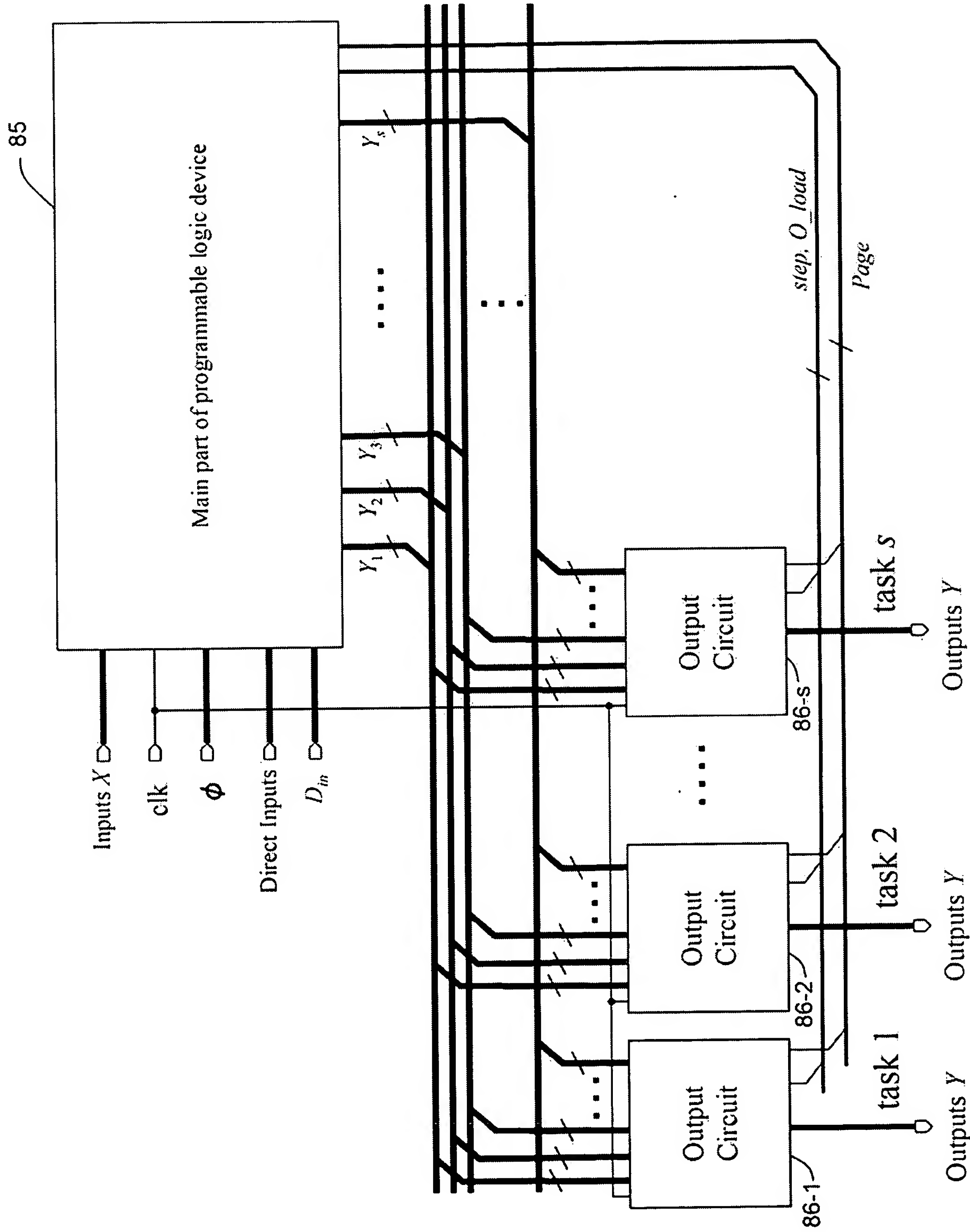
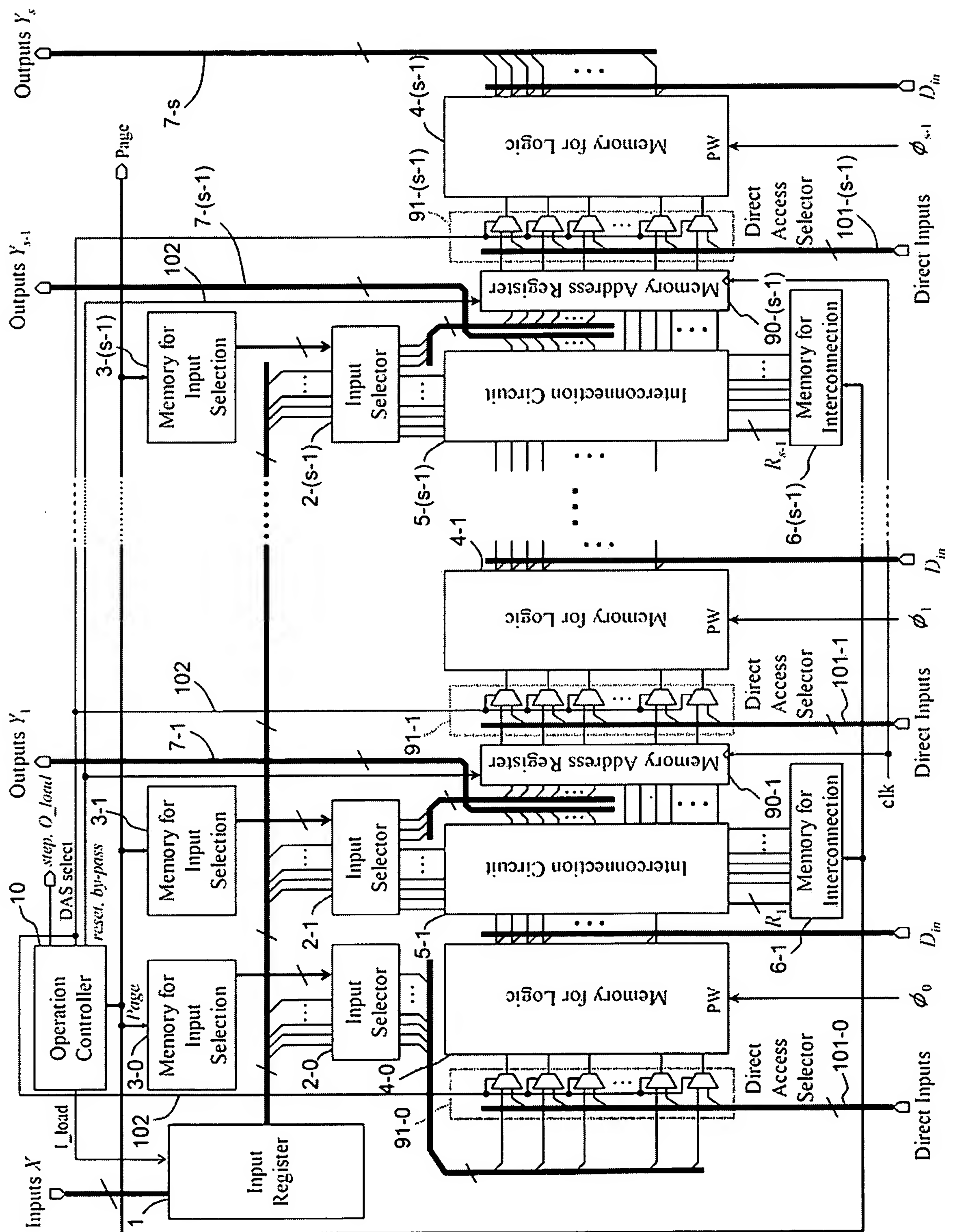


FIG. 39



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FIG. 40



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FIG. 41

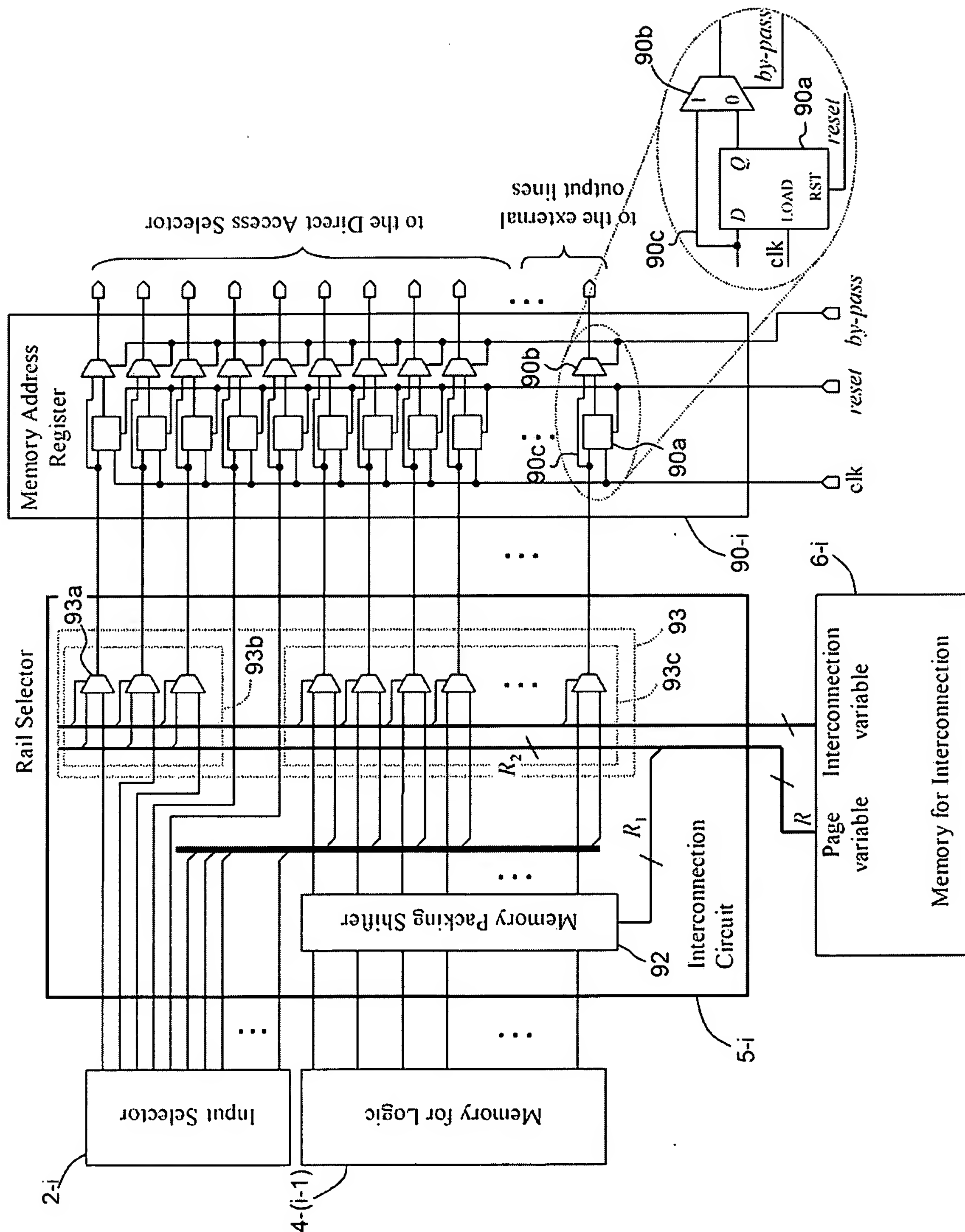
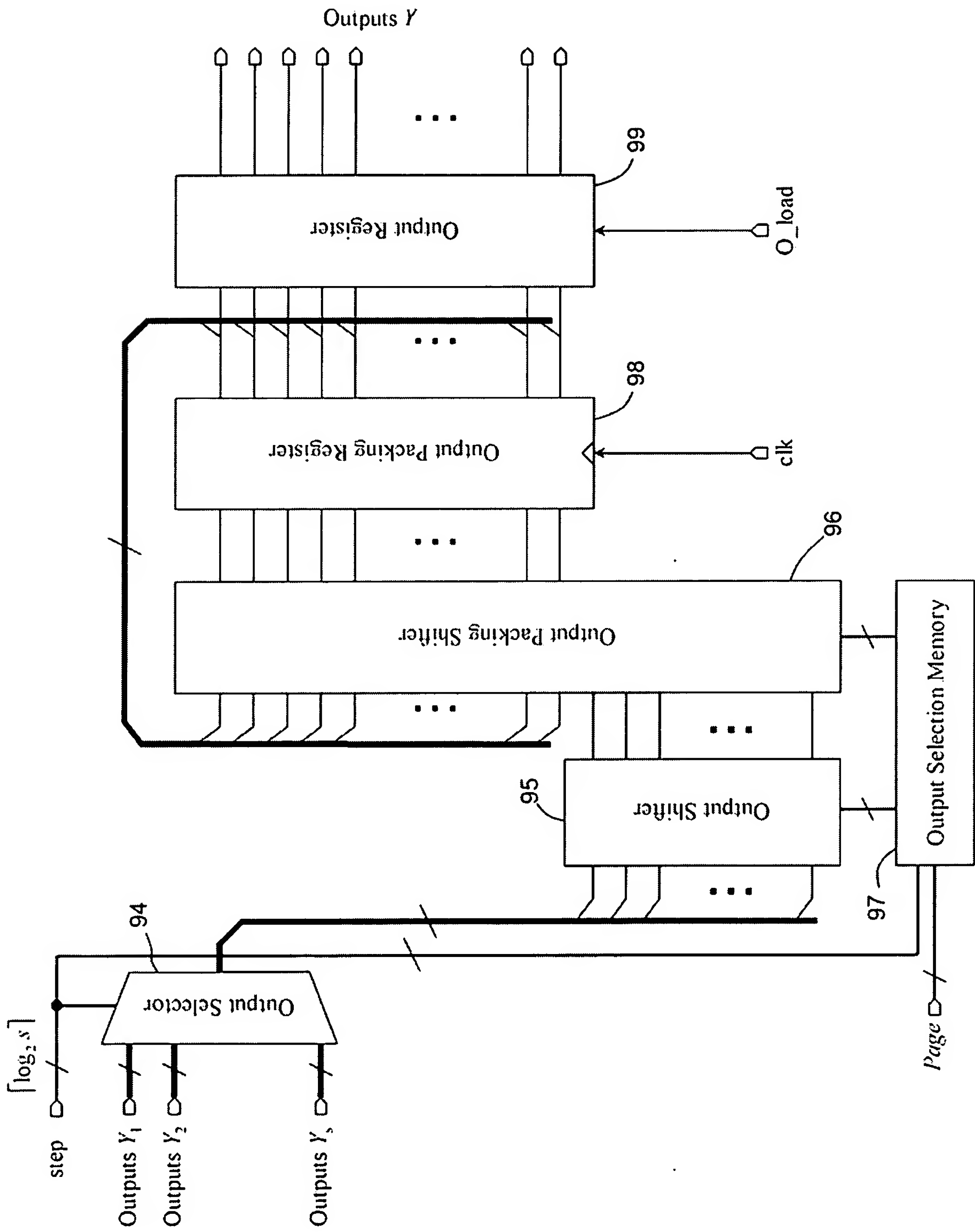
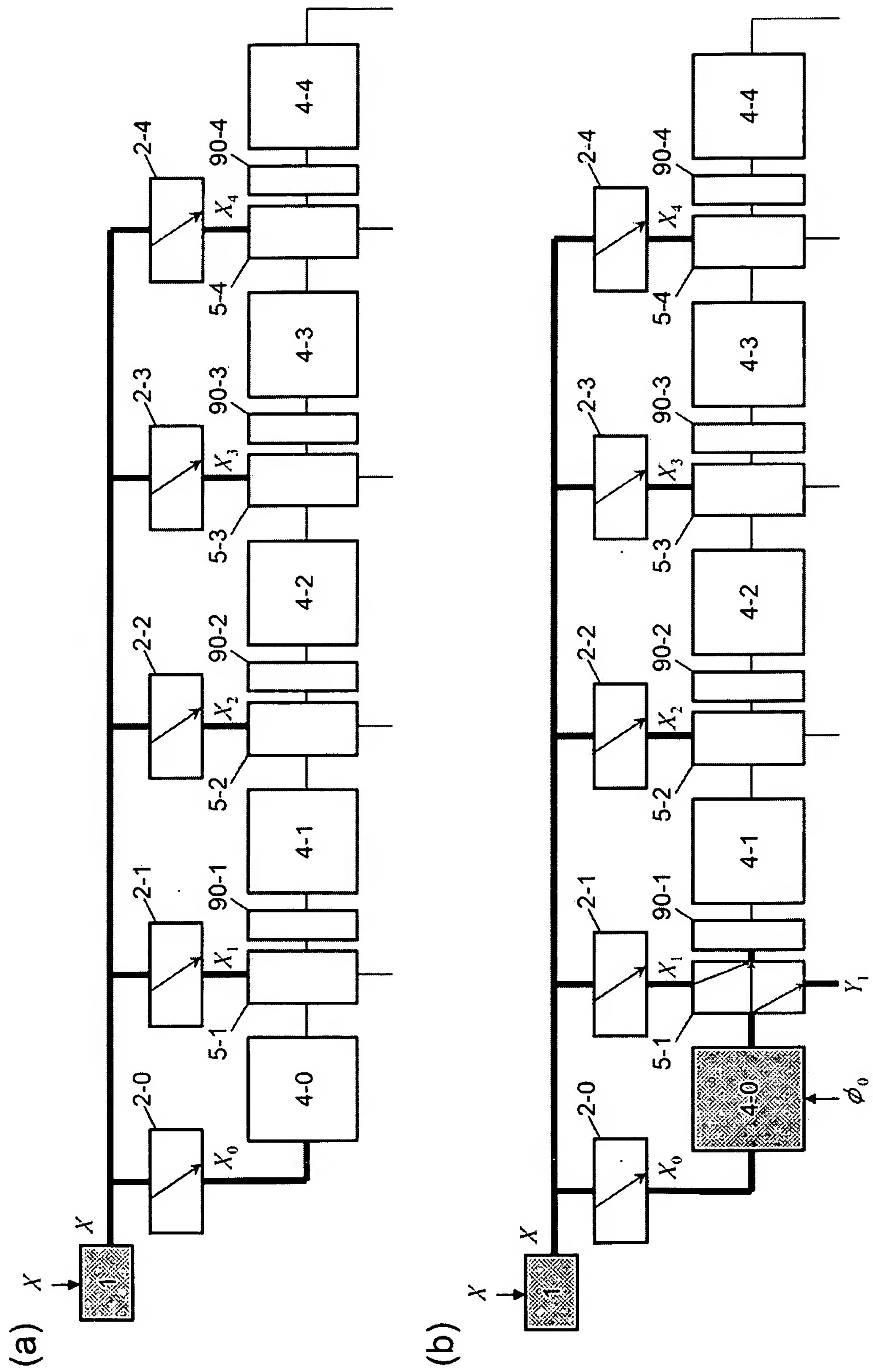


FIG. 42



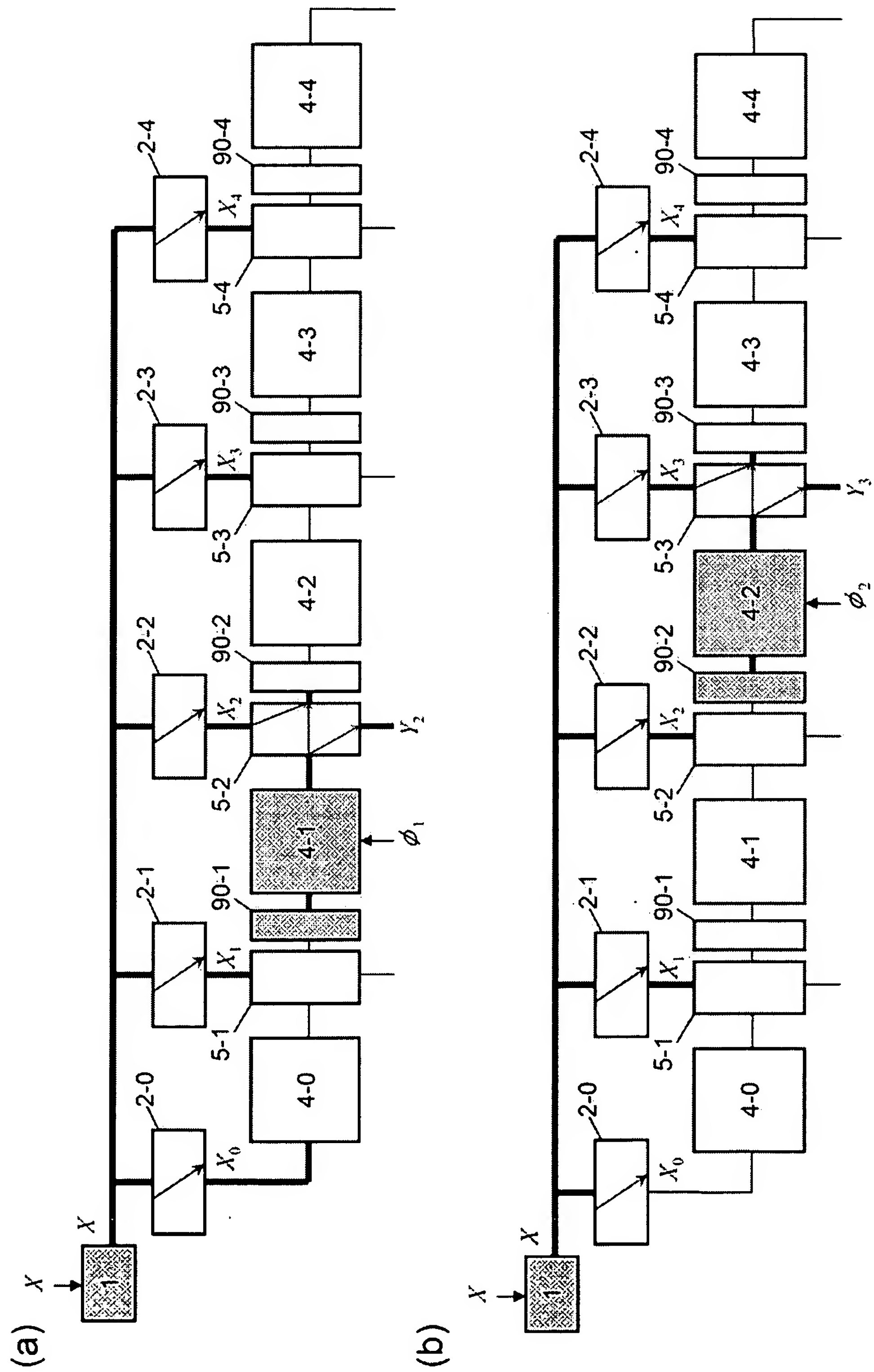
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FIG. 43



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FIG. 44



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FIG. 45

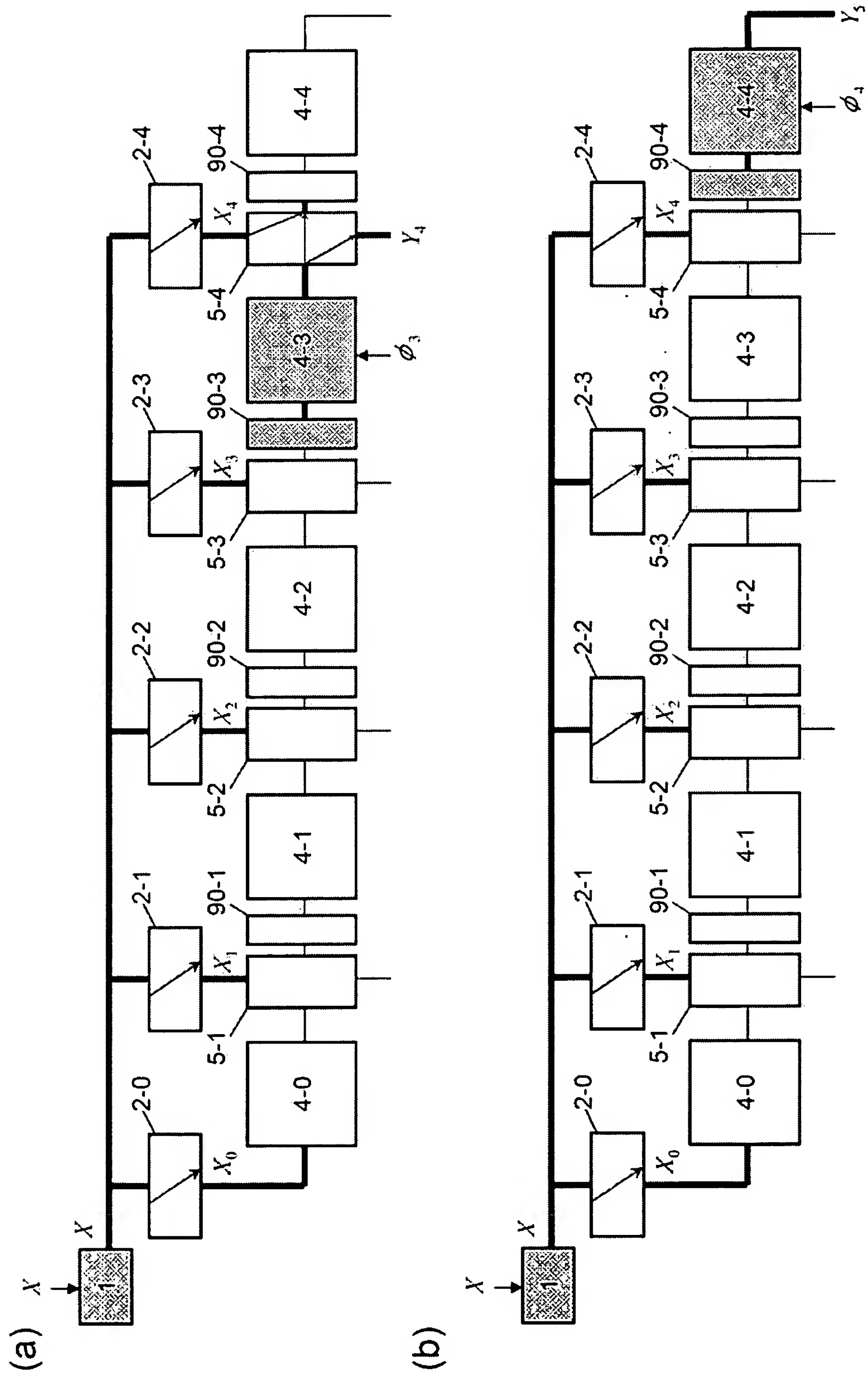
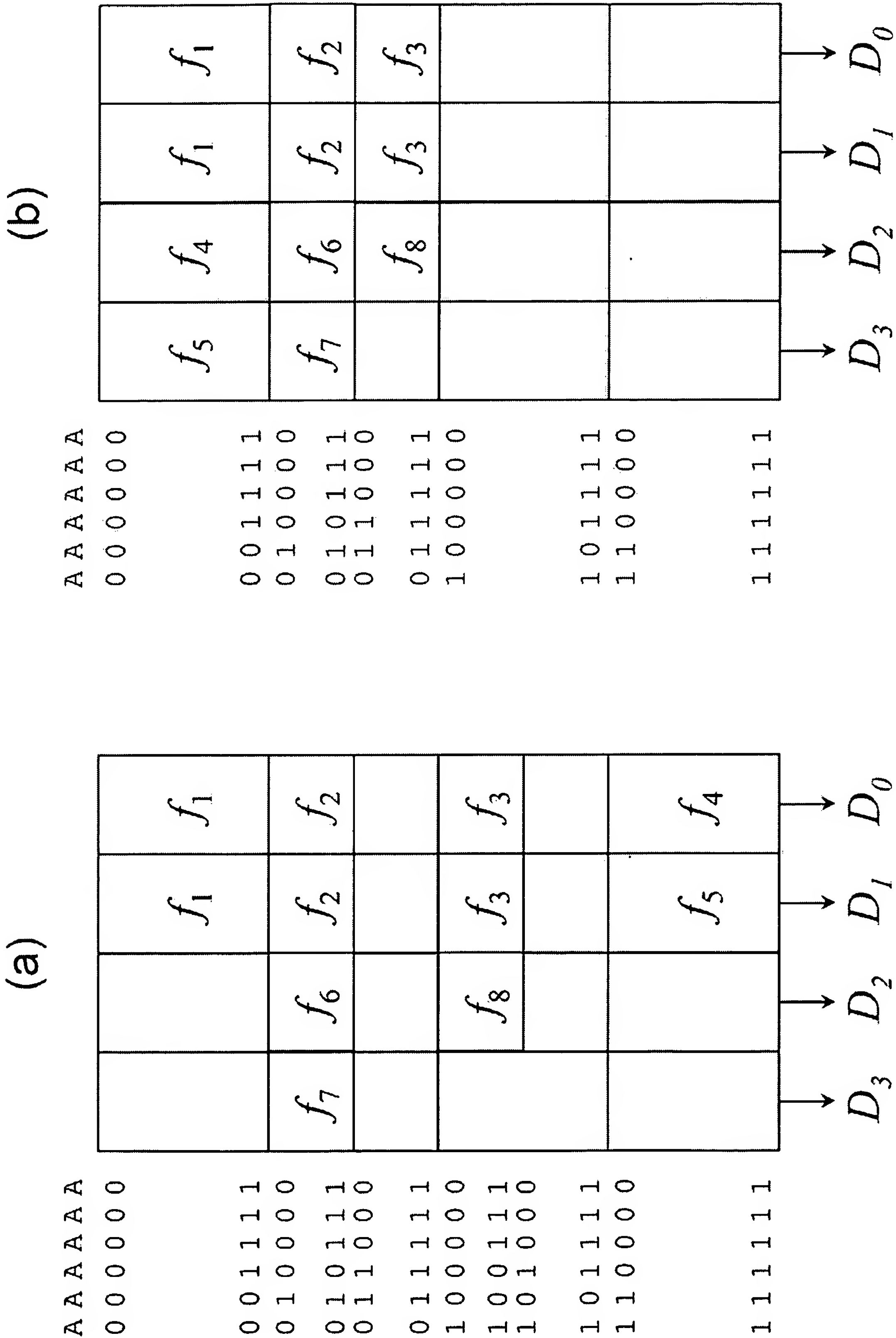


FIG. 46



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FIG. 47

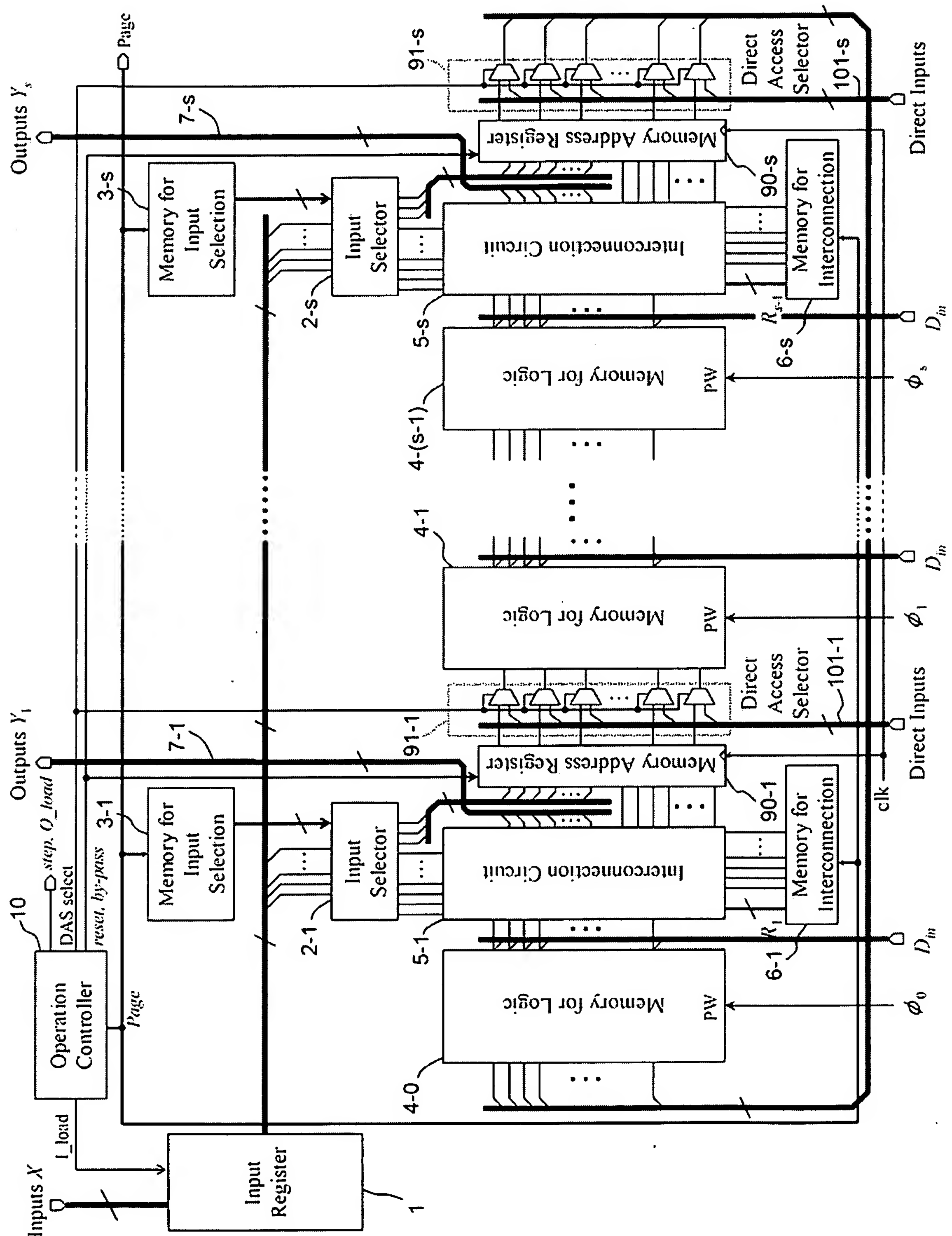


FIG. 48

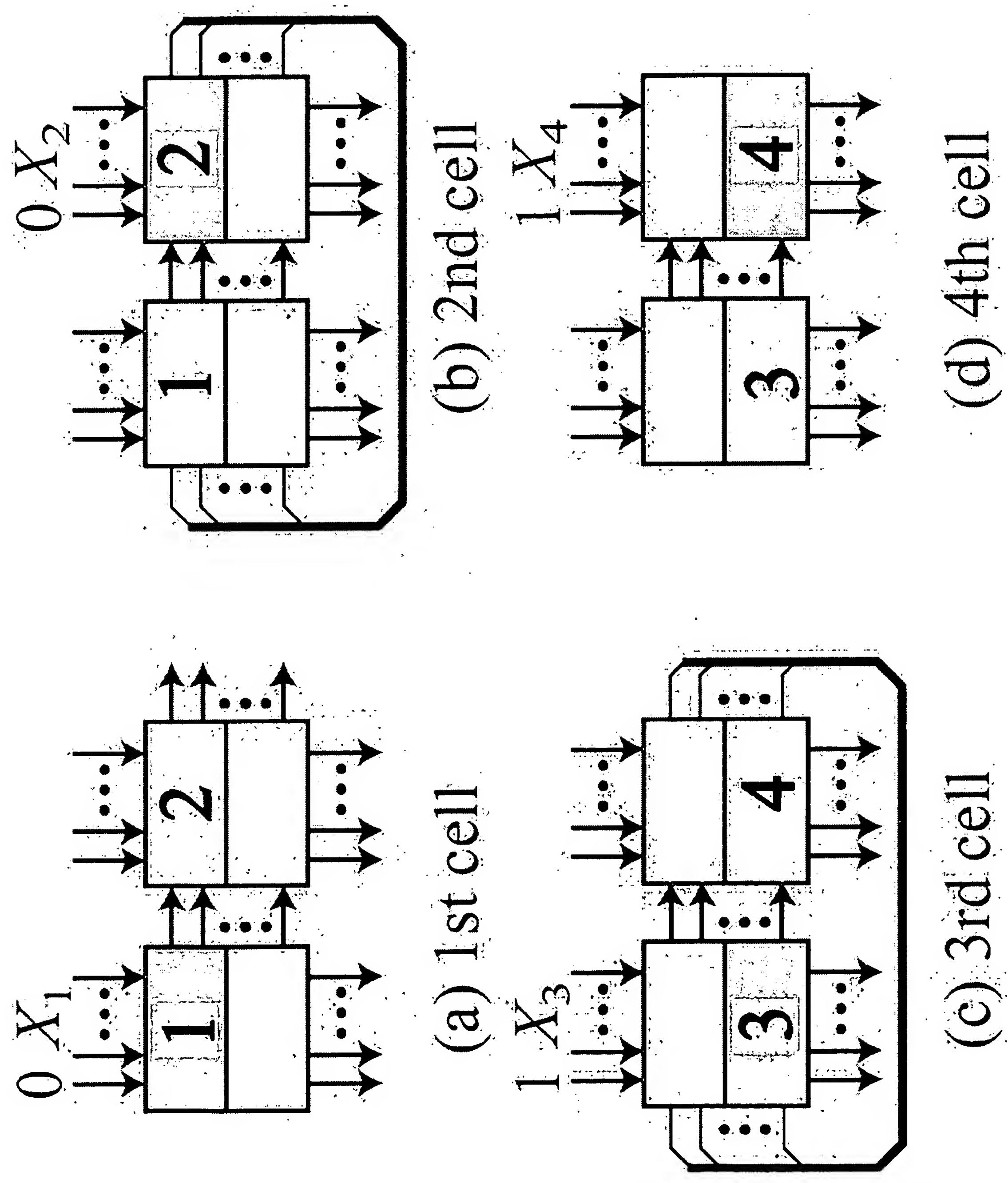
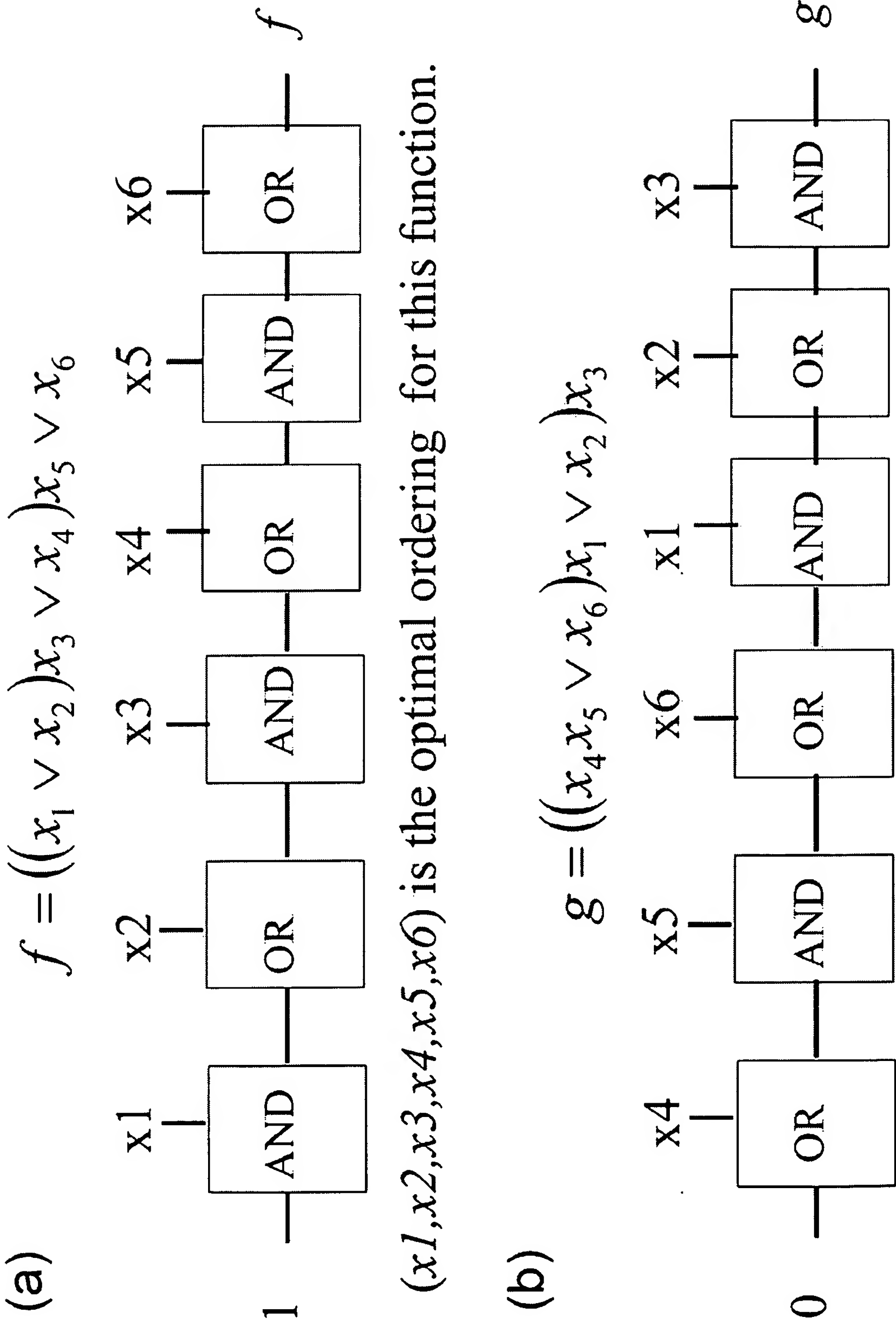


FIG. 49



$(x1,x2,x3,x4,x5,x6)$ is the optimal ordering for this function.

(b)

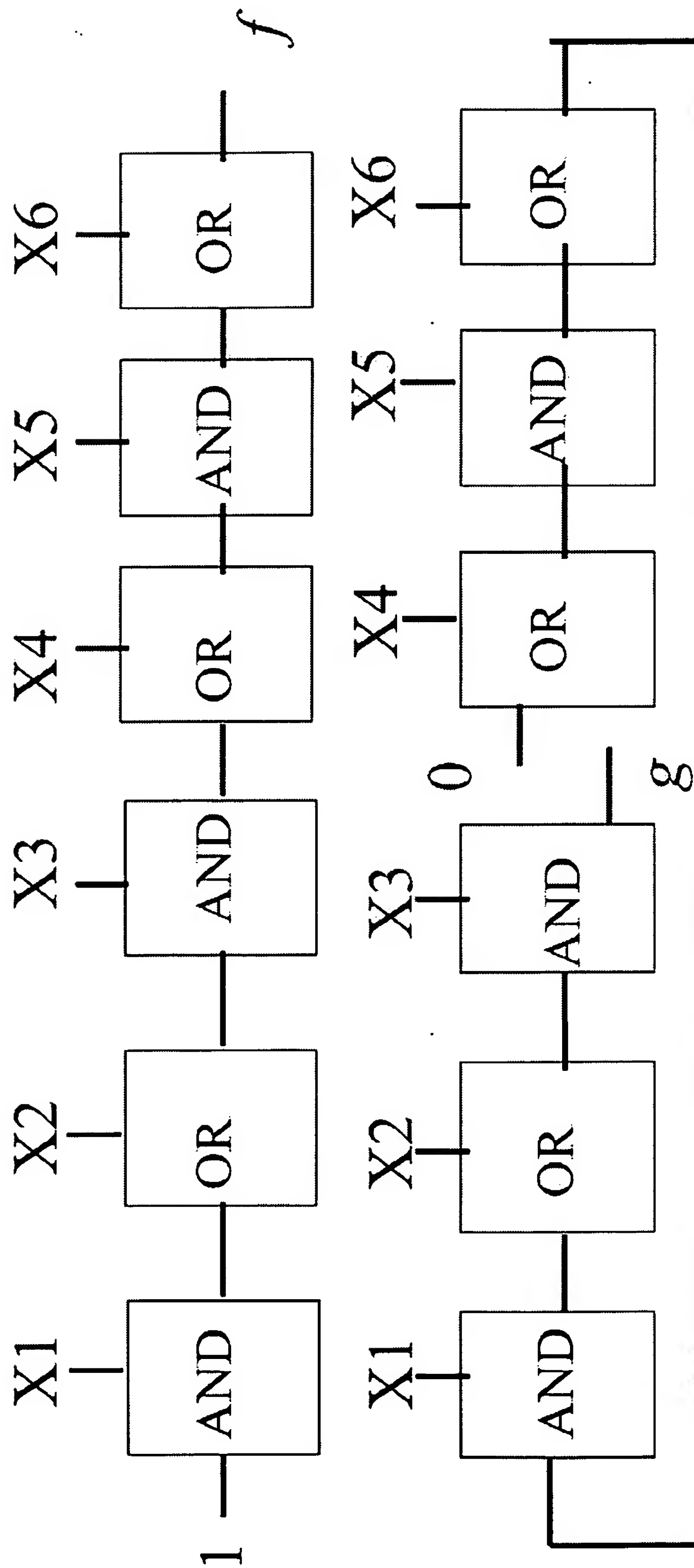
$(x4,x5,x6,x1,x2,x3)$ is the optimal ordering for this function.

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FIG. 50

$$f = ((x_1 \vee x_2)x_3 \vee x_4)x_5 \vee x_6$$

$$g = ((x_4x_5 \vee x_6)x_1 \vee x_2)x_3$$



$$f = ((x_1 \vee x_2)x_3 \vee x_4)x_5 \vee x_6$$

$$g = ((x_4x_5 \vee x_6)x_1 \vee x_2)x_3$$

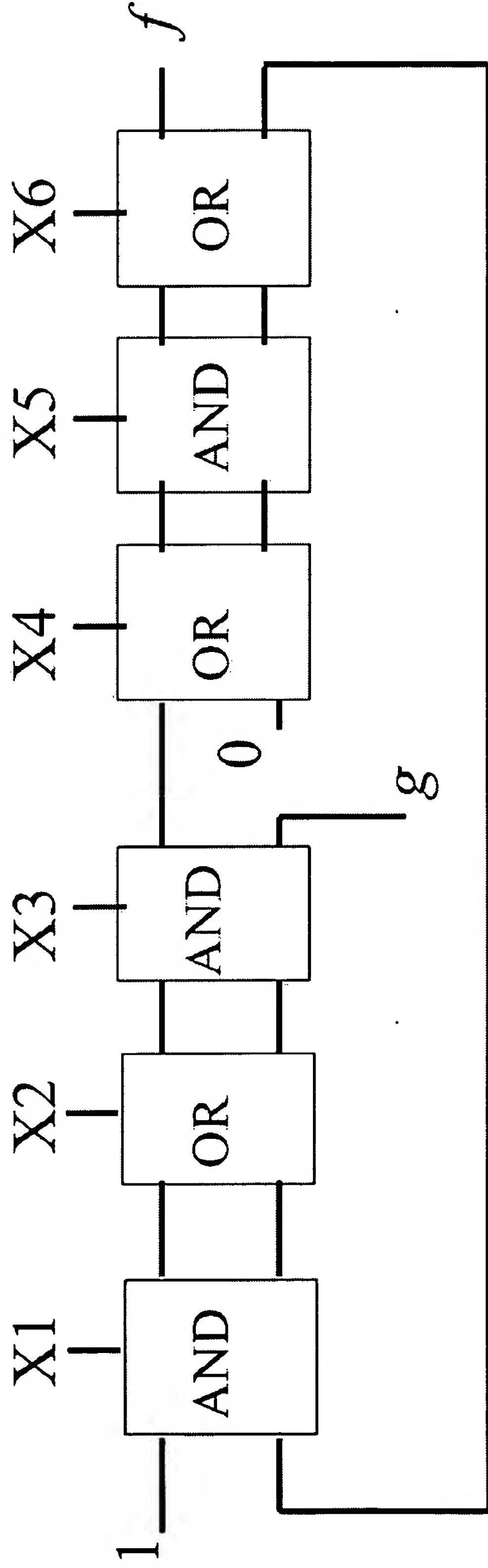


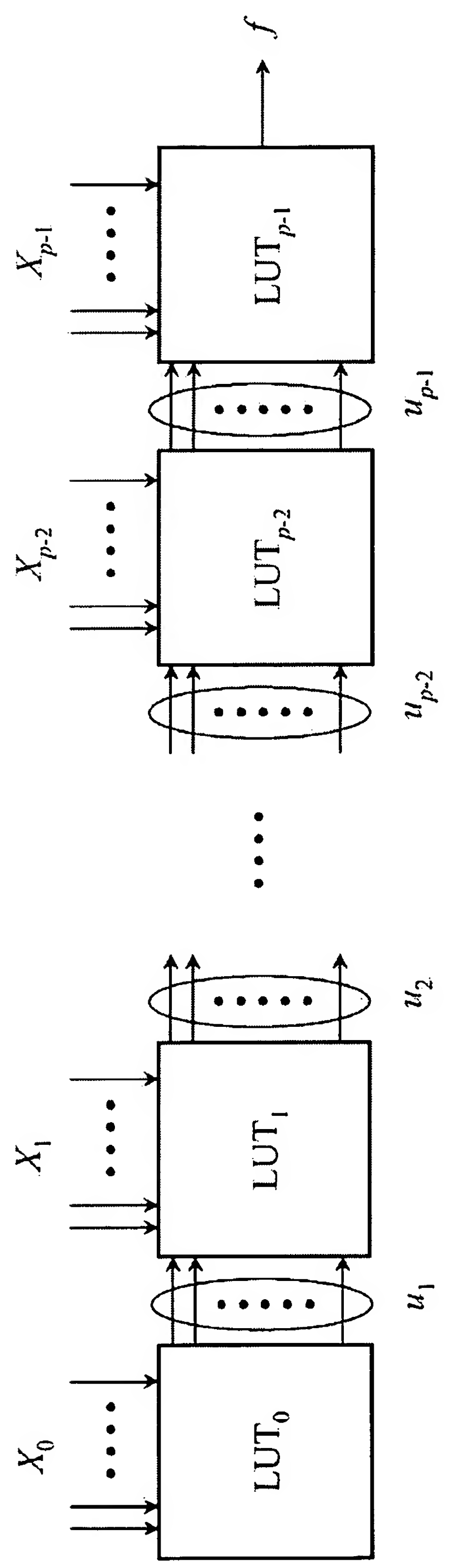
FIG. 51

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By using the LUT ring, the ordering can be optimal for two functions.

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FIG. 52



LUT cascade with p memory cells